Order Number 8814014

Multilevel interconnection technologies—a framework and examples

Pai, Pei-Lin, Ph.D.

University of California, Berkeley, 1987

U·M·I

300 N. Zeeb Rd.
Ann Arbor, MI 48106

Multilevel Interconnection Technologies-A Framework and Examples

By

Pei-Lin Pai

B.S. (National Taiwan University) 1981
M.S. (University of California) 1984

DISSERTATION

Submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

ENGINEERING

in the

GRADUATE DIVISION

OF THE

UNIVERSITY OF CALIFORNIA, BERKELEY

Approved: W G Oldham Sept 30, 1987
Chairman Date

David Boume Sept 30, 1987

Paul K. Ko Oct. 5, 1987

DOCTORAL DEGREE CONFERRED
DECEMBER 15, 1987

Multilevel Interconnection Technologies-A Framework and Examples

Pei-lin Pai

Abstract

Multilevel interconnection is widely practiced today ; however the difficulties in the metal patterning and topography planarization processes motivate more research in interconnection technology. An additive thin-film patterning process (LOPED) is examined , and a planarization process using spin-on glass is investigated. The metallization process in general is studied, and those approaches that can be extended beyond VLSI are selected for more detailed study.

(I) Thin-film patterning:

A new lift-off process using edge-detection (LOPED) can pattern thin films deposited with good step coverage. Some guidelines, including a process window , have been developed for the LOPED process to assure successful patterning. The potential of this process is demonstrated for both metallization and trench isolation. In the lifting step of the LOPED process, acetone penetrates into the patterning resist with a constant speed, leaving a swollen region behind a sharp boundary. The penetration velocity is related to the metal deposition time and volume increase.

(II) Planarization:

Both the current planarization processes using spin-on glass (SOG) are severely challenged when the underlying metal pitch approaches 2.5μm. unless a sandwich structure (SOG/LTO/SOG) is used. The material properties needed for successful applications of SOG are investigated. Infrared spectrophotometry shows that the concentration of hydroxyl and organic groups are sensitive to the annealing conditions. The stress levels of SOG films on Si wafers are always low (less than 10^8Pa in tensile). A strong correlation between the dielectric properties and the OH content in the film is established. SOG IC1-200 (Futurrex Company) shows low dielectric constants and high breakdown fields after 400°C annealing.

(III) Metallization framework:

A general examination of the metallization process shows that, under some practical assumptions, there are thirteen ways to construct a metallization process. Out of the thirteen ways, six do not require planarization after interconnect patterning and are considered promising for VLSI and beyond. Selective metal deposition, e.g. electroless plating, is required by all six approaches. Electroless-plated Ni and Pd may be used for via filling and Cu for interconnects. A buried metal process, either using lift-off or electroless plating, can provide a planarized surface after metallization.

W G Oldham

William G. Oldham

Chairman

Table of Contents

List of Figures

List of tables

Acknowledgements

During the four years of research, I have owed much to many people that I cannot possibly list them all here. The following is just an abbreviated list with the apology to the many that have been omitted.

Above all, I am indebted to Professor William G. Oldham. I can never overstate the importance of his guidance and support on this work. It has been a privilege to work with him. I also wish to express my gratitude to Dr. Yosi Shacham-Diamand. Together we enjoyed the excitement of developing and implementing new ideas.

My thanks go, too, to Professor Ping Ko for his invaluable discussion, Professor Andrew R. Neureuther for his help in simulation, and Professor David Soong of the Chemical Engineering Department for his help in polymer chemistry.

It has been my pleasure to work with those talented members of my research group. In particular, I would like to thank Ginetto Addiego, Carl Galewski and Pantas Sutardja for their support and friendship during the past four years.

Also, I would like to thank the managers and technicians of the Berkeley Microfabrication laboratory. Without their help, this work would never be done. Katalin Voros and Bob Hamilton have gone out of their ways to help me in the laboratory. Marilyn Kushner, Kim Chan, Tom Booth, Robin Wallace and Robert Norman also gave me their indispensable help. It has been a great pleasure working with them in the laboratory.

I have benefited enormously from the summer work at Intel Corporation in 1986. I am most indebted to Dr. Chiu H. Ting for his help and guidance on the spin-on glass work. I would also like to thank Robert Root and Shaw-Yi Lin for their friendship.

This work was supported by the National Science Foundation and the Joint Service Electronics Program

Chapter 1
Introduction

Interconnection is an essential part of modern microelectronics technology. It is needed to deliver power and signals to the circuit, and is also needed to output the processed signals off the chip. In addition, interconnection allows communication between devices and subsystems as needed to perform the desired functions. For VLSI and beyond, the circuit complexity requires multilevel interconnection, which can save the valuable chip areas for active devices [1] (Fig.1.1) and improve the circuit performance by reducing the time delay from long wiring [2]. Multilevel interconnection can also simplify the routing procedure for chip layout by providing more options to the designers. As a result, multilevel interconnection is widely practised today. In this research, several subjects in multilevel interconnection technology are addressed, including thin film patterning, dielectric planarization and a general treatment of the options in a fully planarized metallization process.

The patterning of conductive films is among the most difficult challenges for dry etching. Examples of such difficulties include low anisotropy, poor selectivity, reliability problems due to corrosion and the etchability problem of non-volatilizable elements associated with aluminum etching. Additive patterning processes present a fundamentally different approach to thin film definition. One of the most widely used additive patterning methods is lift-off. However, the poor step coverage required by traditional lift-off process is in conflict with the requirements of VLSI. In chapter 2, a lift-off process using edge-detection (LOPED) is investigated as an alternative thin-film patterning process for etching. This technique can be used with non-overhanging resist profiles and with thin films that are conformally deposited. The applications of the LOPED process in metallization and trench isolation show the potential in VLSI and beyond.

Current interconnection technology is limited to two or three layers of metal films [3,4], with a few exceptions of four layers in bipolar processes [5]. The resolution of the first metal layer is usually between 3.0μm to 4.0μm (pitch), and may be reduced to 2.0μm pitch in the

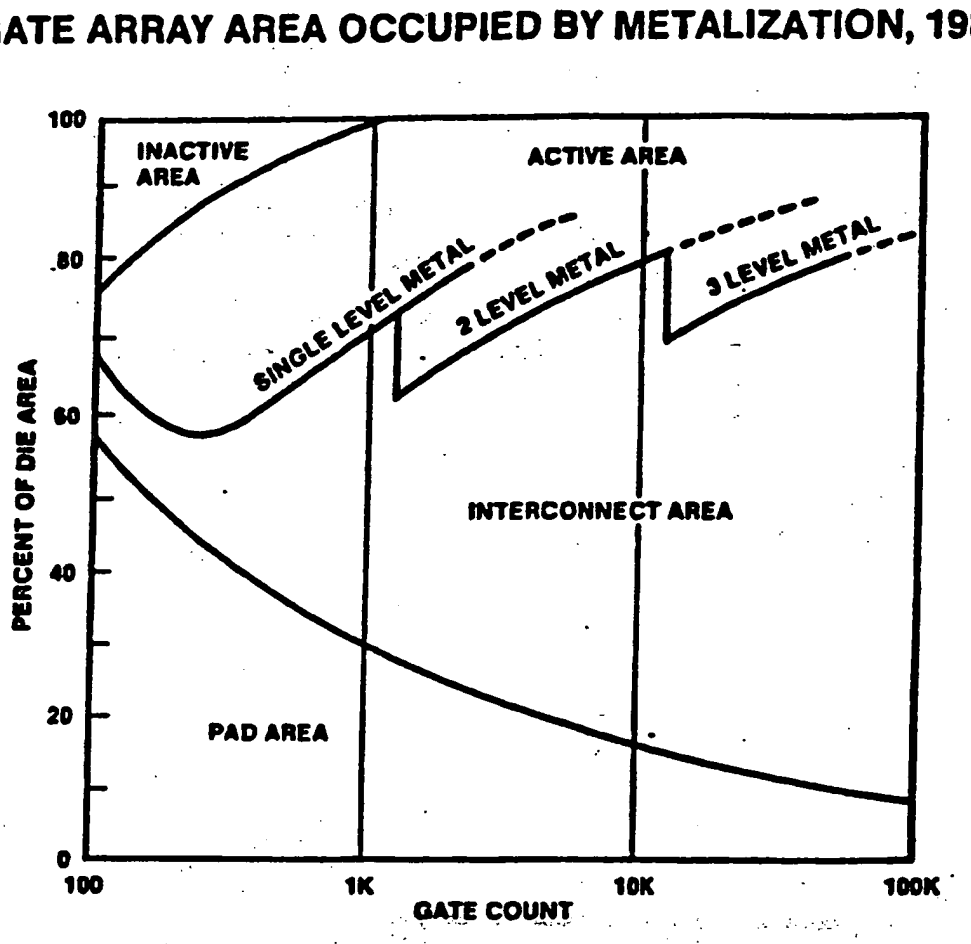


Figure 1.1 Relative area occupied by devices, interconnects and pads in gate arrays [1].

near future. The resolution of the second layer is about 4.0μm to 6.0μm (pitch), and is aimed at 3.0μm for the next generation technology. The key limiting factor is the topography generated by each process step. After the dielectric film and the metal film are patterned, sharp steps prevail on the surface. If not planarized, these sharp steps can lead to severe step coverage problems in the following deposition - the metal films can be exceedingly thin along the bottom corners of the steps. In addition, the metal film deposited on the sidewalls is difficult to etch completely, resulting in residual film (or "stringers") along the foot of the steps. Chapter 3 examines one of the planarization techniques: the use of spin-on glass (SOG). The etch-back approach is found inadequate for high-resolution metallization processes. The simple non-etchback (SOG/LTO) can sometimes lead to severe topography, and the sandwich structure (SOG/LTO/SOG) can provide a smooth surface for the next deposition. The material properties of several SOGs are studied and a process to obtain good electrical properties of SOG is developed.

Surface topography, when accumulated over several layers, can eventually limit the resolution of optical lithography. The resolution of a lithography system with an illuminating light of wavelength λ and a numerical aperture N.A. is [6]:

$$w = \frac{k\lambda}{N.A.} \tag{1}$$

where w is the minimum feature size and k is an empirical constant depending on the resist and processes. The depth of focus for this system is [6]:

$$D.F. = \frac{\lambda}{2(N.A.)^2} \tag{2}$$

If equation (1) is put into equation (2) to replace the N.A. term, the depth of focus is expressed in terms of the resolution limit and the wavelength:

$$D.F. = \frac{w^2}{2k^2\lambda} \tag{3}$$

For a 2.0μm pitch (w = 1.0μm) with k = 0.8 and λ = 0.436μm, the depth of focus is only 1.8μm. A 3.0μm pitch (w = 1.5μm) with the same parameters results in a depth of focus of 4.0μm. Most MOS processes generate about 0.5μm to 1.0μm topography on the substrate

surface before metal deposition (from the polysilicon gate and the isolation process.) The photoresist needs about 0.5μm tolerance to assure good resolution. These two factors use up more than 1.0μm of the depth of focus, and leave less than 1.0μm tolerance for the 2.0μm pitch and less than 3.0μm for the 3.0μm pitch. Each metal layer will generates a surface topography of about 0.8μm to 1.0μm. As a result, current lithography technology is severely challenged at the 2.0μm pitch for the second metal layer and at 3.0μm pitch for the third layer. One way to avoid this limitation is to develop a global planarization process for metallization. In chapter 4 a general survey of the multilevel interconnection technology is given. Thirteen metallization processes, which include most practical cases reported in the literature, are discussed. Six of the processes do not require planarization and are proposed for future work as the base process for multilevel metallization.

Reference

[1] A.N. Saxena, D. Pramanik, " Manufacturing Issues and Emerging Trends in VLSI Multilevel Metallizations," *IEEE VLSI Multilevel Interconn. Conf.*, 9(1986).

[2] V. Ramakrishma, A. Oberai, P. Farrar, D. Kermeter, " Future Requirements for High-Speed VLSI Interconnections," *IEEE VLSI Multilevel Interconn. Conf.*, 27(1987).

[3] M.J. Thomas, W.T. Cochran, A.S. Harrus, H.P. Hey, G.W.Hills, C.W. Lawrence, J.L. Yeh, " A 1.0 Micrometer CMOS Two Level Metal Technology Incorporating Plasma Enhanced TEOS," *IEEE VLSI Multilevel Interconn. Conf.*, 20(1987).

[4] H.M. Naguib, C. Jang, T.F. Klemme, K. Wong, A. Rangappan, W.W. Yao, R.T. Fulks, " The Evaluation and Development of Planarization Technique for Double Level Metallization in 1.2 Micron CMOS Technology," *IEEE VLSI Multilevel Interconn. Conf.*, 93(1987).

[5] T.A. Bartush, " A Four Level Wiring Process for Semiconductor Chips," *IEEE VLSI Multilevel Interconn. Conf.*, 41(1987).

[6] L.F. Thompson, M.J. Bowden, 'The Lithographic Process: The Physics,' *Introduction to Microlithography*, ed. by M.J. Comstock, American Chemical Society, 1983.

Chapter 2

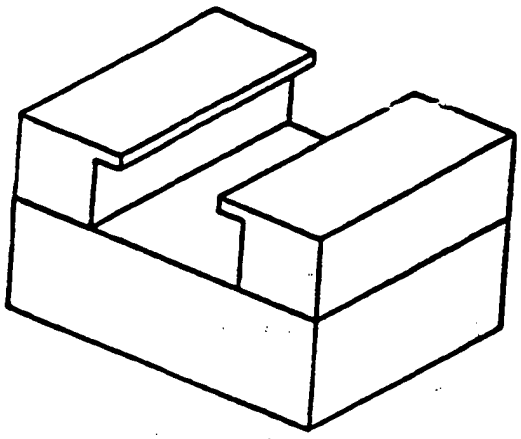
A Lift-Off Process Using Edge-Detection (LOPED)

2.1 Introduction

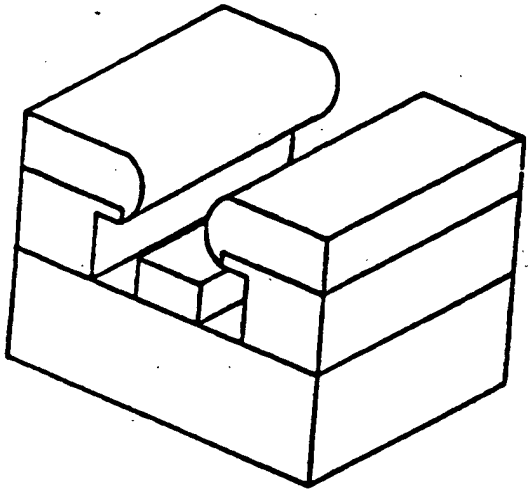
Traditional metal patterning processes are severely challenged in the VLSI era. Dry etching involves tradeoffs of selectivity, etch rate, uniformity and anisotropy. Furthermore, the addition of copper in the aluminum alloy to increase the electromigration resistance aggravates the selectivity problem and can lead to residues since Cu does not form volatile compounds in chlorine-based plasma chemistry. Additive thin-film patterning is a fundamentally different approach that does not have the above-mentioned problems.

Examples of additive patterning processes are selective deposition and lift-off. Selectively-deposited tungsten is being widely explored as an alternative to aluminum [1,2]. Tungsten has a higher resistivity (6 - 10 μΩ-cm) than aluminum (2.7 - 3.0 μΩ-cm), but can sustain a much higher temperature (above 1000°C) than Al (lower than 600°C). Consequently, BPSG reflow at 800° - 1000°C can be used for planarization after the metal deposition. However, W does not adhere to oxide well and the fluorine-content from the source gas (WF_6) may corrode the underlying silicon substrate. The deposition also requires special equipment and a rather complicated process cycle. Despite more than 5 years of research and development, selective tungsten is not yet widely accepted for production.

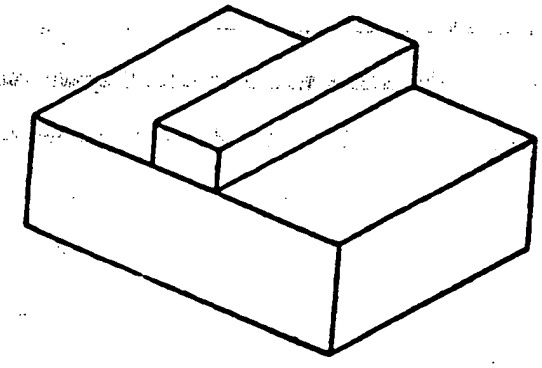
Lift-off is another technique for patterning of thin-films (Fig.2.1). It has been occasionally used in medium- and large-scale integration technologies because of low-cost and simplicity[3-22]. The lift-off technique is capable of patterning any film deposited at a low temperature (lower than the hardening temperature of the underlying medium) and has infinite selectivity to the underlying substrate. The principal limitation of the technology stems from the fact that the directional deposition required by the process is in conflict with step coverage requirements. In fact with certain assumptions Homma showed that traditional lift-off techniques are limited to metal pitch larger than 2.5μm [23]. Lift-off is practiced by few



(a)



(b)



(c)

Figure 2.1: Process flow of direct lift-off. (a) a lyer of photoresist is patterned by a dark-field mask and processed to form a reentrant angle. (b) the desired thin film is deposited with poor step coverage. (c) the lift-off process is completed by dissolving the lifting medium in a solvent. The excess film is removed at the same time.

manufacturers.

In this chapter, the lift-off process is more carefully examined. The problems due to inadequate process design are separated from the fundamental limits. A new edge-detection method is used to extend the lift-off process to sub-VLSI dimensions, and the process window for manufacturing is studied . Applications in both metallization and trench isolation are demonstrated. The interaction between photoresist and some solvents are also studied usig the edge-detection method.

2.2 Experimental Setup

For most experiments, p-type (100) Si wafers are used as the substrates. If surface topography is needed, Si wafers are patterned by photolithography and plasma-etched in a LAM AutoEtch 410 system. The etching conditions and characteristics are summarized in P.L. Pai's master report, " Trench Technology Using Low Temperature CVD Oxide and Lift-Off." Glass wafers are used when inspection through the back is needed. The glass wafers are much thicker (around 2mm) than normal silicon wafers (around 0.5mm), and most automatic equipment in the laboratory cannot operate on the glass wafers.

Both Kodak820 and AZ1400-series resists have been used as the patterning photoresist. Abundant information on this resist has been collected and its performance is evaluated regularly. The thickness of this resist spun at 4600 rpm is around 1.1μm after 120°C baking. An Eaton automatic wafer track coats this resist onto the wafers with a controlled acceleration, spinning speed and spinning time. The wafers are transferred to a hot plate after coating on a moving belt. The temperature of the hot plate is set at 120°C and the baking time is usually 60 seconds. Another "cool plate" next to the hot plate can lower the substrate temperature to room temperature before loading to the receiving cassette. AZ1400-series resists are coated on a Headway manual spinner. The spinning speed and time are adjustable on this machine. After the resist coating, the wafer is either put on a hot plate at 90°C - 95°C for a minute or put into an oven at the same temperature for 15 minutes. The thickness of the resist depends on the solids content and the spinning speed. Two most widely used resists are AZ1400-31 and

AZ1400-21. The former resist has a thickness around 1.6μm for a 3000 rpm spinning speed. This thick resist is usually used when severe topography exists. The AZ1400-21 resist is about 0.6-0.9μm thick after coating and is used when submicrometer features are desired.

A GCA 6200 stepper is used for exposure. This system is a g-line (λ = 436 nm) 10X stepper with a numerical aperture of 0.28. For most applications, this system can resolve 1.25μm lines and spaces routinely. When higher resolution is needed, an overexposure can push the resolution down to 0.8μm lines and spaces. An exposure matrix is used to determine the optimal exposure time and focus before each exposure job. The glass wafers are too thick for the stepper and a Kasper contact printer is used to expose the wafers. The resist-coated sides of the wafers are in contact with the Cr side of the mask. A Hg-lamp then exposes the resist through the mask.

Kodak820 resist is developed in the 932 1:1 developer from the KTI Company. An MTI omnichuck spreads the developer over the wafer automatically. The process steps are programmed through a terminal. The development time is usually set to 60 seconds, followed by a spin dry cycle. For the AZ resist or glass wafers, immersion development is used. AZ developer (1:1 diluted) or AZ 351 developer (diluted 5:1=AZ 351:H_2O) can develop the AZ resist within 60 seconds. The wafers are usually blown-dry by a nitrogen gun after the development.

A well-controlled resist etch is critical to the process described in the following section. The etching is also used in a descum step, which removes the resist residues to improve the critical dimension control. At the end of the lithography step, a good resist stripping process is also needed to result in a clean, residue-free surface. Several resist etching processes have been tested, and O_2 plasma treatment seems to give the most consistent results for all these applications. A Technics plasma etching/deposition system is used for this purpose. This system can generate a 30 KHz plasma in the process chamber. As shown in Fig.2.2 the etch rate for a 300 mTorr O_2 plasma is linearly related to the power:

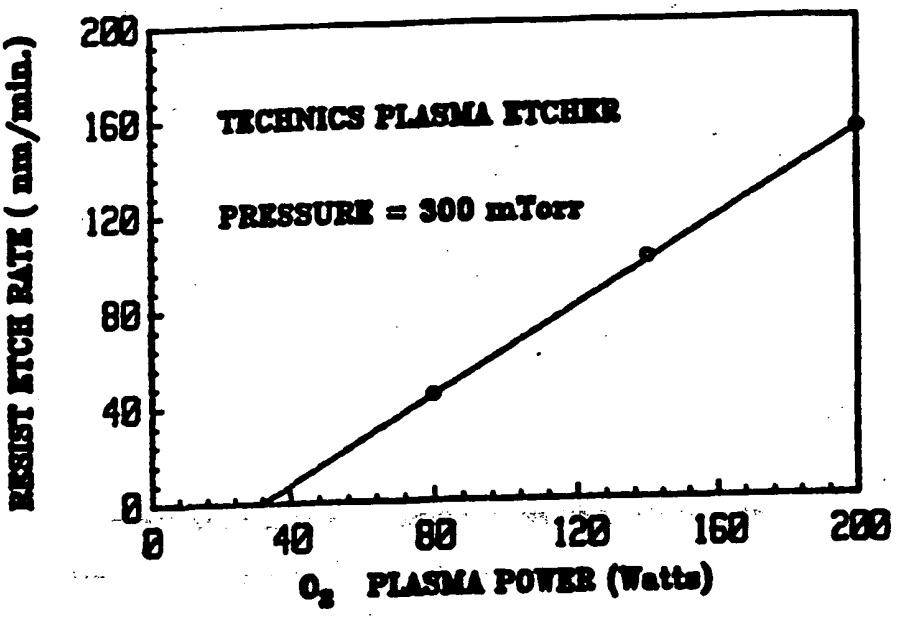


Figure 2.2: The etch rate of photoresist in O_2 plasma.

$$R_{O_2} = 0.91 \times (\text{Power} - 32) \quad \text{nm/min.} \qquad (1)$$

A 140-Watt plasma can remove 100 nm, or 0.1μm, photoresist per minute. The uniformity of this etching is within +/- 10% across the chamber. This process is used for both the controlled etchback and descum step. To strip the resist, a high power (e.g. 300 Watts) O_2 plasma can be used. Or more frequently, a piranha solution ($H_2SO_4 : H_2O_2 = 6:1$) or an acetone bath is used. Pirahna is a strong oxidizing solution and attacks the Al films; consequently it is only used before the first metal layer. Acetone is an organic solvent that can remove photoresist. A more detailed study of the acetone/resist interaction will be given in section 2.5. If the photoresist is hardened, e.g. by plasma etching or ion implantation, acetone cannot remove the resist completely. Either O_2 plasma stripping or a proprietary resist stripper is in need. The resist stripper PRS-1000 can remove most hardened photoresist unless the exposure time to a high power plasma exceeds 15 minutes. In that case, only the O_2 plasma or the piranha solution can effectively remove the resist.

Two sputtering systems are used to deposit Al-1%Si films. One is a d.c.-plasma sputtering system from the Sputtering Film System Corp.. This is a single-wafer deposition system with a 6-inch EMCA-6 target about 5cm from the wafer. A maximum of 6 wafers can be loaded into the the chamber and sequentially rotated into the sputtering position. The base pressure for this system is about 7×10^{-7} Torr. The conformality of the deposition is improved by a rotating magnetic field within the plasma. For a 1KW plasma, the deposition rate is about 0.2μm/min.. The other system is an a.c.-plasma sputtering system from the Circuits Processing Apparatus, Inc.. As many as 9 wafers can be loaded onto a pallet at a time. About 20 pallets can be stored at the sending station and processed later. The deposited film thickness is controlled by the time the wafers are exposed to the plasma. Due to the double load-lock system, the base pressure within the process chamber is always kept below 4×10^{-7} Torr.

2.3 The edge-detection method

The key steps of the lift-off process using edge-detection [20,22-23] are shown in Fig.2.3

for a metal film example. First a layer of photoresist is patterned using a dark-field version of the metal mask (Fig.2.3(a)). The resist in the areas to receive metal is exposed and developed out. A standard optical-lithography process is used here and no resist shaping procedures are needed. Then the desired thin film is deposited on the wafer (Fig.2.3(b)). The metal film deposition technology is not restricted to processes with poor step coverage - in fact we use a sputtering source with excellent step coverage. An additional layer of resist is spun over the deposited film (Fig.2.3(c)). The fact that the spun-on film is thinnest in the vicinity of sharp edges permits a simple method of edge detection. A controlled etchback is used to selectively break through this thinnest part of the spun-on layer (Fig.2.3(d)) (although photoresist is used for convenience, it is not exposed, and its photo-sensitive properties are irrelevant.) This etch-back step is carefully timed so that on the one hand a gap is produced at all edges, but on the other hand the remaining areas are still protected. A second isotropic etching step is used to selectively attack the exposed regions of the deposited film and reveal the edge of the pattern-ing resist (Fig.2.3(e)). This step is timed to just clear the sidewalls. The LOPED process is completed by the lifting step; all the resist, together with the excess metal film, is removed by soaking in an organic solvent (Fig.2.3(f)).

The coating of the top layer resist and its etching are critical to the success of the LOPED process. If the resist is too thin or overetched, there may be no resist left to protect the desired metal patterns; if the resist is too thick or underetched, there may be no opening to the deposited metal films at the corners. Similarly, the etching step which removes the metal sidewalls (through the gap) is critical in determining process viability. In the following we estimate the combined allowed ranges of the key variables to generate the manufacturing pro-cess window.

2.4 Process window for the LOPED process

One measure of the viability of a process for manufacturing is the volume in process

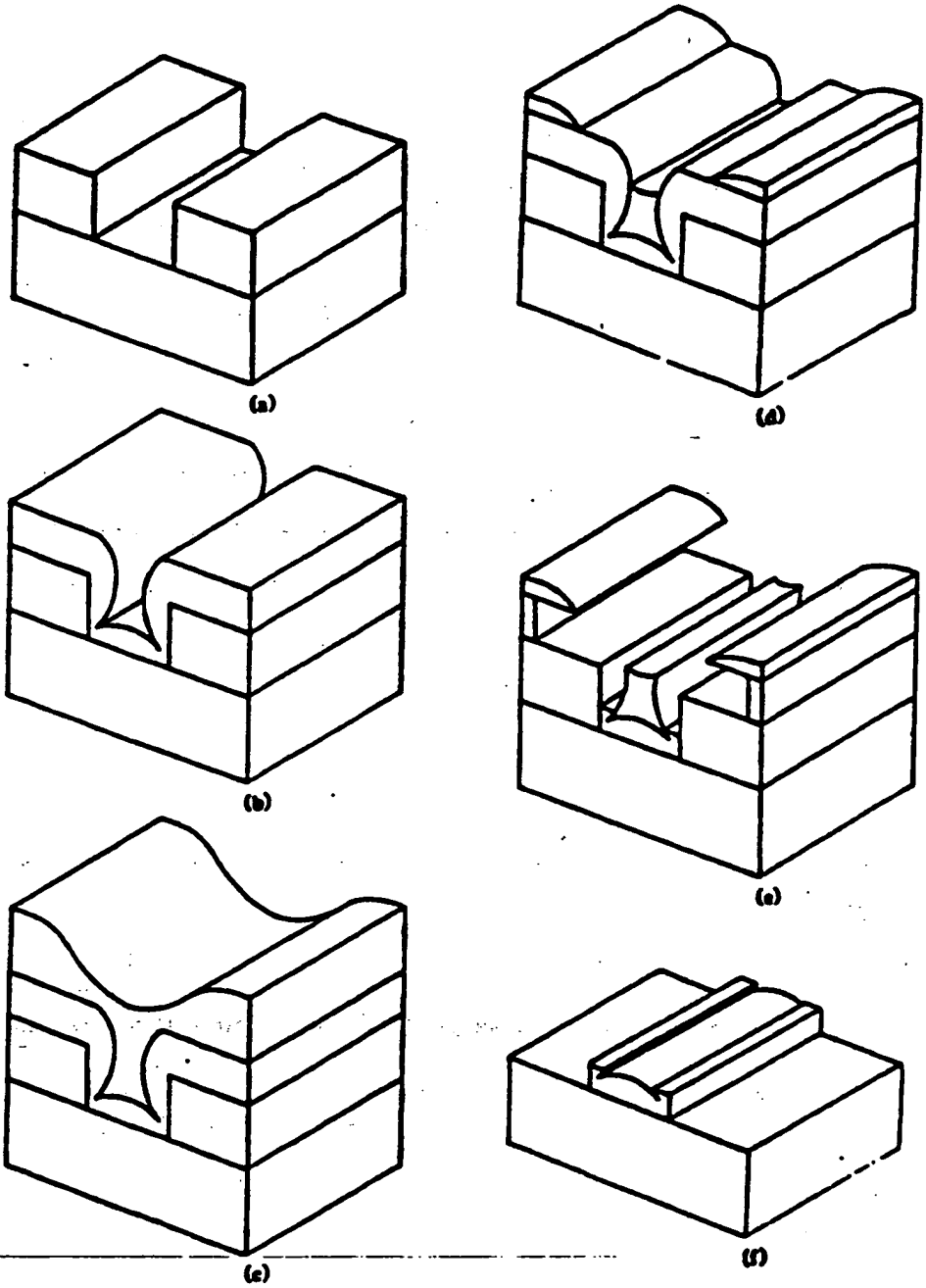


Figure 2.3: The outline of the LOPED process. (a) a layer of resist is patterned by a dark-field mask and flood exposed after development. (b) the desired thin film is deposited with good step coverage. (c) a second layer resist is applied. (d) the second layer resist is etched. (e) the deposited film is etched. (f) the lift-off process is completed.

parameter space for which the process specification is met. Two dimensional sections of this volume are referred to as the process window. For the LOPED process the principal parameters are the thicknesses of the various films, the etch depths in the two etching steps, and the dimensions of both the desired metal patterns and the underlying topography. In the following two sections we first evaluate the relationships between the various film thicknesses and then derive some process window examples for the most important control parameters, the extent of the two etch back steps.

Edge-detection constraints. - It is possible to estimate the constraints on the resist process used for edge detection using a conservative approximation. We assume that the spun-on film is nearly flat in the vicinity of an edge during the early stage of spinning and volume shrinkage determines the final profile. Fig.2.4(a) shows the cross-section of a normal application, in which a metal pattern of width W is patterned by the sidewalls of the patterning resist with thickness R1. The thickness of the top layer resist is R2 before shrinkage. The drying process changes the resist thickness to k×R2 (k < 1). After the etching of the top layer resist, at least part of the metal film deposited on the corners of the patterning resist must be exposed as shown by the dotted line. However, it is essential that a step in the topography underlying the metal not result in detection of a false edge. An example is shown in Fig.2.4(b), in which a sharp step (H) is within a large metal pattern. The underlying metal film should not be exposed during etchback. The top layer resist is conservatively assumed flat near the step before shrinkage. The resist thickness over a lower level near the step edge (e.g. point A) is (R2 + H). After shrinkage, the resist thickness at this point is k×(R2 + H). The resist etchback is defined by the fraction k′ of the flat-field resist thickness (k×R2) which is removed. The resist thickness remaining at point A is

$$k\times(R2 + H) - k'\times k\times R2 \qquad (1)$$

A conservative condition to assure that no metal film is exposed can be derived by assuming that the remaining resist at point A should be thicker than the step height H as shown in the

dotted line in Fig.2.4(b):

$$k \times (R2 + H) - k' \times d \times R2 > H \tag{2}$$

The requirement on the dried resist thickness $k \times R2$ can be derived by rearrangement:

$$k \times R2 > \frac{(1-k) \times H}{(1-k')} \tag{3}$$

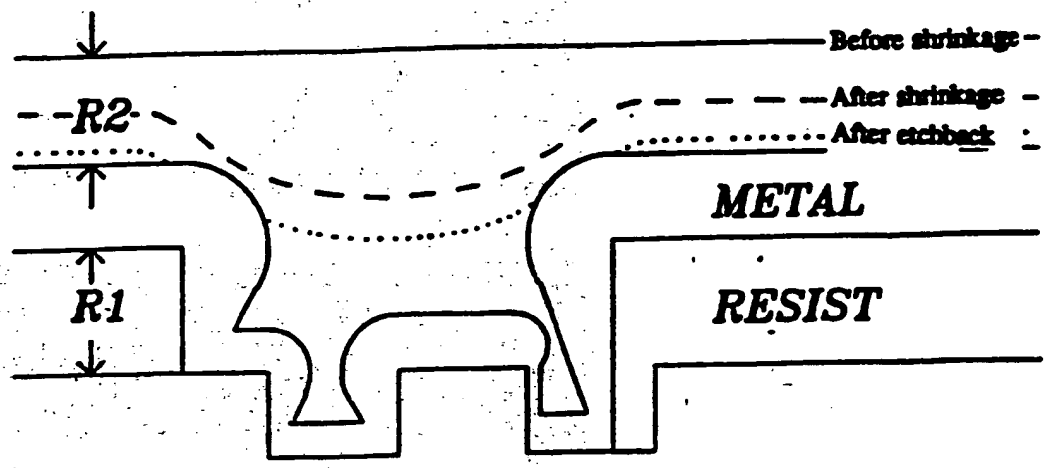
The thinning effect also constrains the thickness of the edge-detection resist layer. As the thickness of the top layer resist increases, the thinning effect around a sharp corner for a fixed R1 decreases. More specifically, a top layer resist thicker than the patterning resist generally leads to insufficient thinning-effect and an inadequate process window. The minimum width of the desired patterns is also an important factor in determining the acceptable range for the top layer resist. Based on an empirical characterization of the spin process we find that the patterning width must exceed the final thickness $k \times R2$. The upper limit for the thickness of the top layer resist is determined by the lesser of the two parameters R1 and W_{min}:

$$\min\left\{R1 \, , \, W_{min.}\right\} > k \times R2 > \frac{(1-k) \times H}{(1-k')} \tag{4}$$

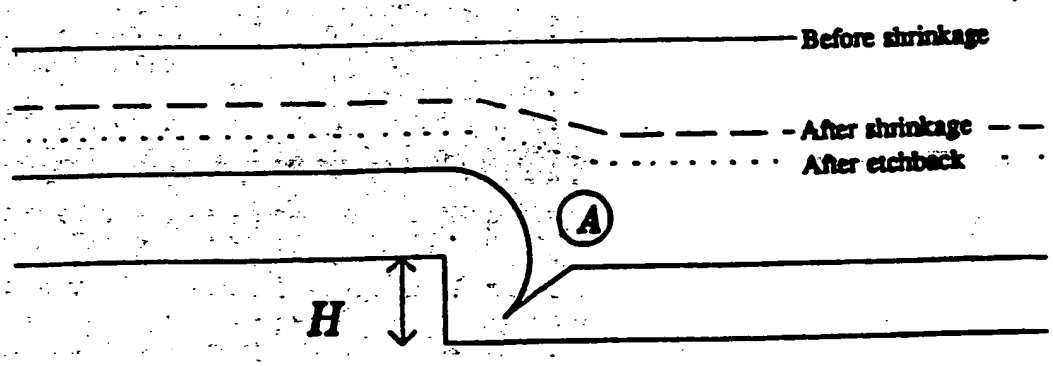
This requirement can be illustrated by a typical example: A 1.1μm (= R1) resist (Kodak820) is used to pattern a 0.7μm thick Al-Si film over a surface topography with 0.8μm steps. The minimum feature size is aimed at 1μm. The shrinkage factor of the top layer resist is estimated to be 50% (= k). In the edge-detection method, 60% (=k') of the top layer resist is etched. The remaining top layer resist (about 0.4μm) is sufficient to cover desired areas without pinholes. The range of the acceptable final thickness for the top layer resist is calculated from equation (5):

$$1.0\mu m > k \times R2 > 0.88\mu m \tag{5}$$

Within this range, a 0.9μm resist can be used as the top layer resist.



(a)



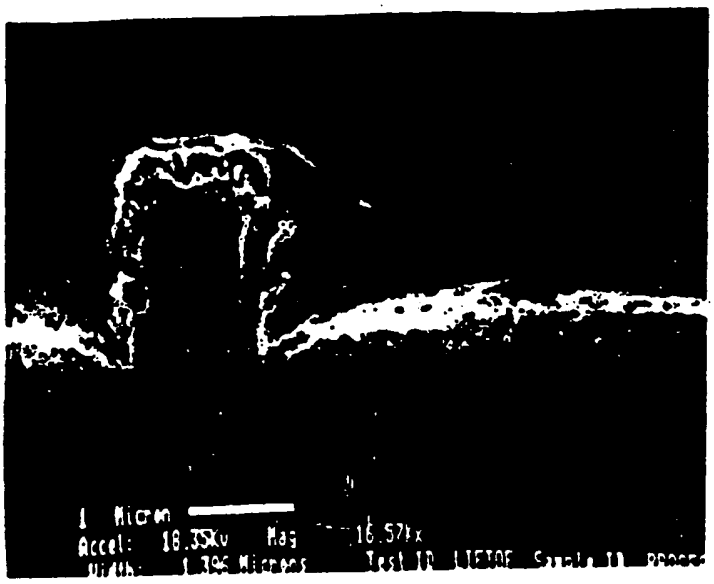
(b)

Figure 2.4: The cross-sections of the LOPED process after the top layer resist coating. (a) For the edge-detection, the top layer resist is thinner around the edges of the patterning resist. (b) The worst case for the edge-detection is to pattern a large metal pattern over a surface step. The metal film deposited at the corner of the step must not be exposed after the etch-back.

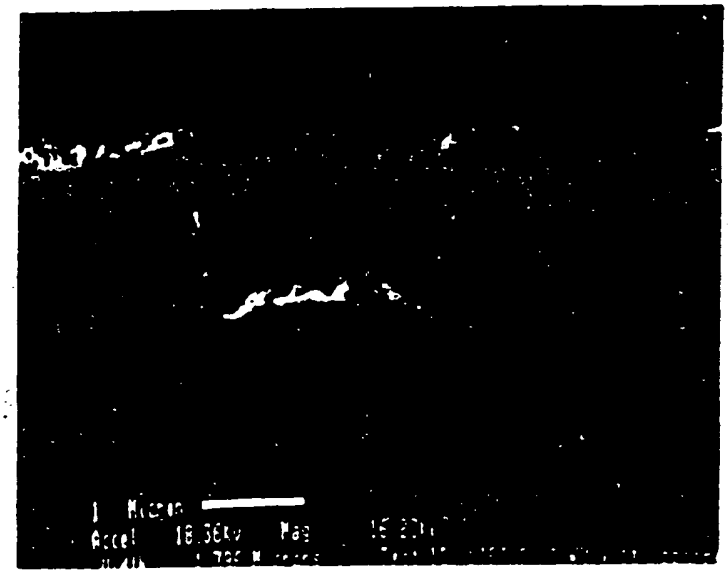
The method described above is useful for a first estimate of the process requirements. The calculation usually gives a conservative prediction; a photoresist thicker than the upper limit or thinner than the lower limit sometimes can also lead to successful results.

Etching requirements. - The geometry of the desired metal pattern is an important factor in limiting the size of the process window. Fig.2.5 shows two examples of patterns at step (c) (Fig.2) of the process flow. In these examples the patterning resist is 1.0μm, the metal film 0.6μm, and the top resist film 0.85μm thick. In Fig.2.5(a) a narrow gap is to be formed in the metal pattern. Because of the narrow line, the top resist is quite thin and only about 10% etchback is needed to open the corners. On the other hand the maximum allowable etchback is limited to about 80% by the requirement for non-zero resist thickness in regions where the metal is to remain (see, e.g. Fig.2.4(b)). From Fig.2.5(a) we may also estimate the constraints on the metal etch for this example. If the top layer resist is just broken through at the corners, then an etchback just equal to the metal thickness is needed to expose the bottom photoresist layer. On the other hand if the top layer resist etchback is more aggressive and exposes the "notch" in the metal corners, only about a 60% metal etch is required. On the other extreme an excessive metal etch will degrade pattern fidelity. For the example of Fig.2.5(a) the allowable overetch varies from 60% (160% total) to 20% (120% total) as the top resist etch goes from the 10% to 80% extremes. These etch limits for the structure of Fig.2.5(a) are summarized in Fig.2.6(a) as a process window. The window of Fig.2.6(a) is for a particular pattern, namely a minimum-width space. If the process window for all possible geometries were plotted on the same co-ordinates, then the intersection would be the actual available process window for simultaneous fabrication of these geometries. Fig.2.5(b) represents the opposite extreme of Fig.2.5(a). The process window of both are plotted in Fig.2.6(b) and the intersection is shown as a hatched region. This region is a reasonable estimate of the actual process window for the LOPEP process with the stated film thicknesses.

A flat surface is assumed in the example calculation of Fig.2.6. If surface topography exists on the substrate, the upper limit of the etchback (k′) is lowered as required by equation

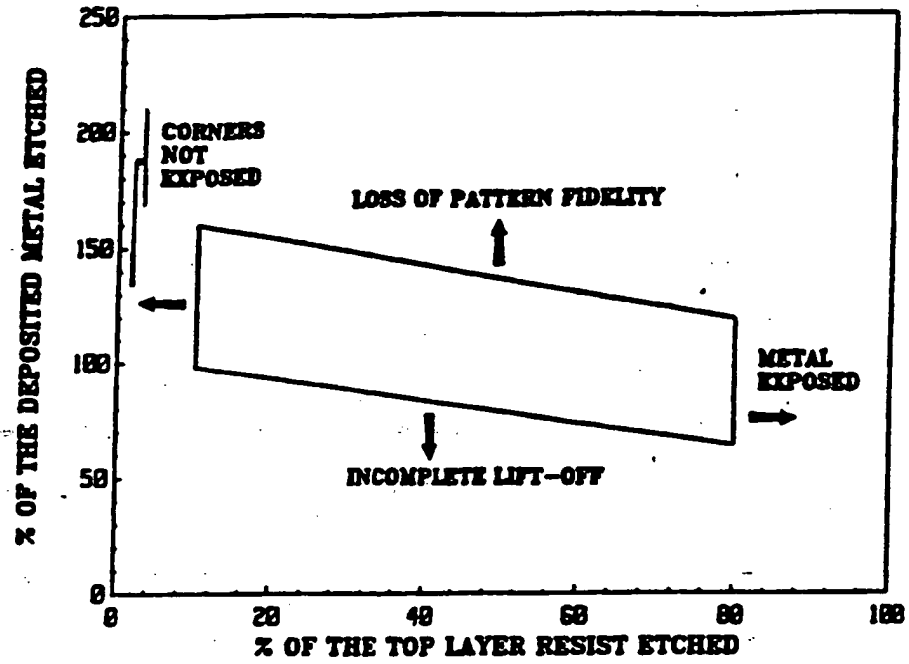


(a)

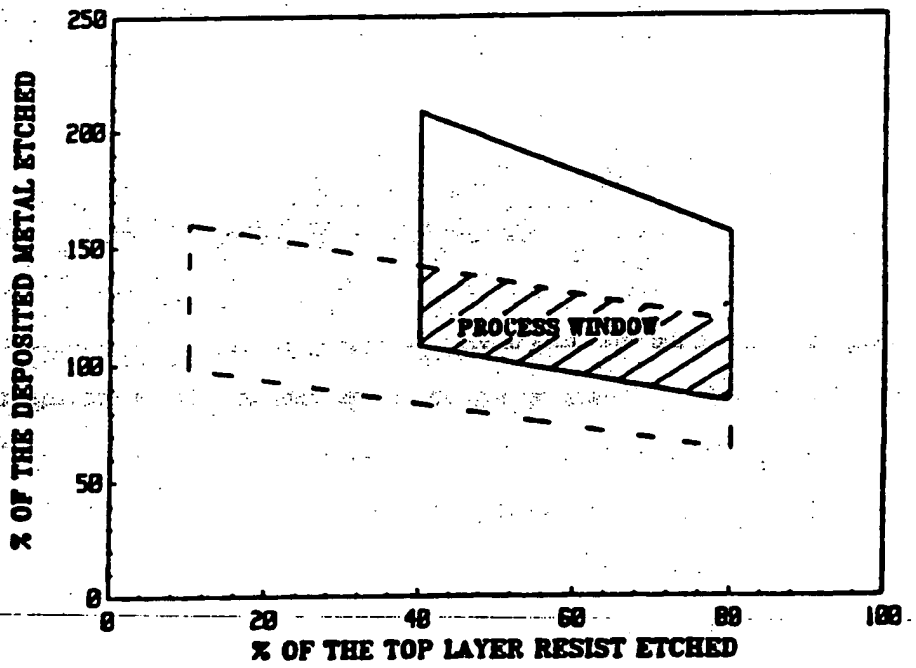


(b)

Figure 2.5: The SEM pictures of the second layer photoresist coated over the substares. (a) The resist is coated over a narrow resist pattern, thus resulting the maximum thinning effect. (b) The resist is coated over a deep trench formed by the underlying resist, and thus the thinning effect is minimized.



(a)



(b)

Figure.2.6: A process window for the LOPED process. (a) The enclosed region is the acceptable ranges for the case in Fig.4(a). (b) The enclosed region is the acceptable range for the case in Fig.4(b). The overlapped region of the windows for the two extreme geometries is the process window of the LOPED process for this combination of film thicknesses.

(4), which is rearranged below:

$$k' < 1 - \frac{(1-k)\times H}{k\times R2} \qquad (6)$$

If the shrinkage factor k for the top layer resist is 50% and the net thickness k×R2 is 0.85μm, then

$$k' < 1 - 0.59 \times H \qquad (7)$$

On a flat surface (H =0), the edge detection method can etch most of the top layer resist (k' < 1). If a step of 0.5μm exists on the surface, the maximum amount of the etchback is limited to 70% (k' < 0.7).

2.5 Applications

The illustrations of the LOPED process have used metal films as the example. We have tested the feasibility of the process, including substrates with underlying topography using standard metallization and resist processing equipment. The topography is generated by etching trenches in the Si wafers. The geometries ranges from 1μm lines and spaces to 10μm lines and spaces with varying step heights. The process, as described, is practiced over the resulting geometries. Fig.2.7 shows an example of an aluminum pattern of 1μm lines and spaces over topography with 0.8μm steps. As can be seen from the SEM picture, the film is continuous across the steps without significant variations in critical dimension. A tapered resist pattern has also been used to test the robustness of the LOPED process. A pattern is formed in 0.7μm of resist with 45° - 50° sidewalls by reducing image contrast. The underlying topography includes steps of 0.6μm in height. The lift-off results are shown in Fig.2.8. Al-Si lines of 1.0μm width are patterned over these steps with good continuity. In the absence of the underlying topography, the GCA stepper can resolve submicrometer features. Fig.2.9(a) shows a pattern of 0.8μm lines and spaces in Al-Si defined by LOPED; Fig.2.9(b) shows another example of 0.6μm lines with 1.0μm spaces. It is also worth noting that this technique works for both large and small geometries. Squares of 2mm by 2mm are patterned on the same substrate with the submicrometer features without difficulty (Fig.2.10). It is clear that the resolution of

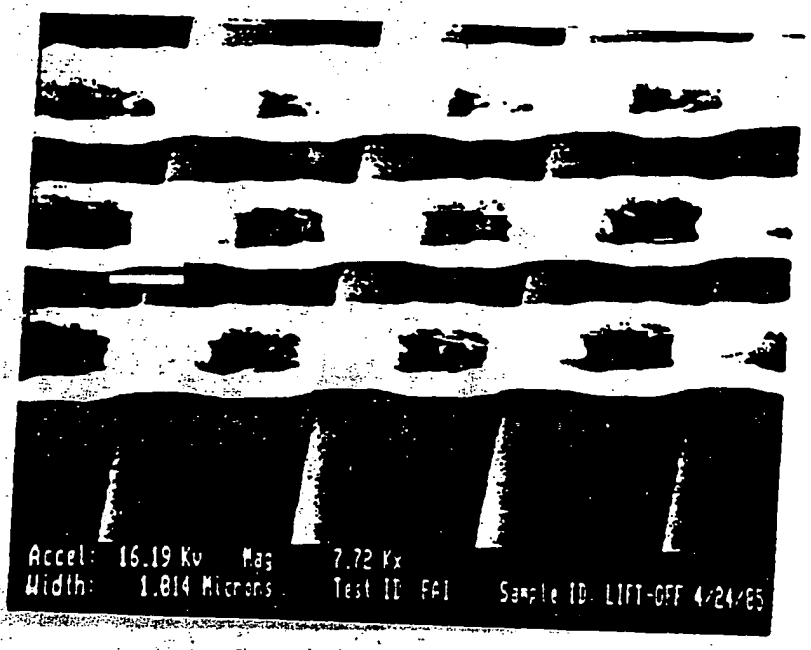
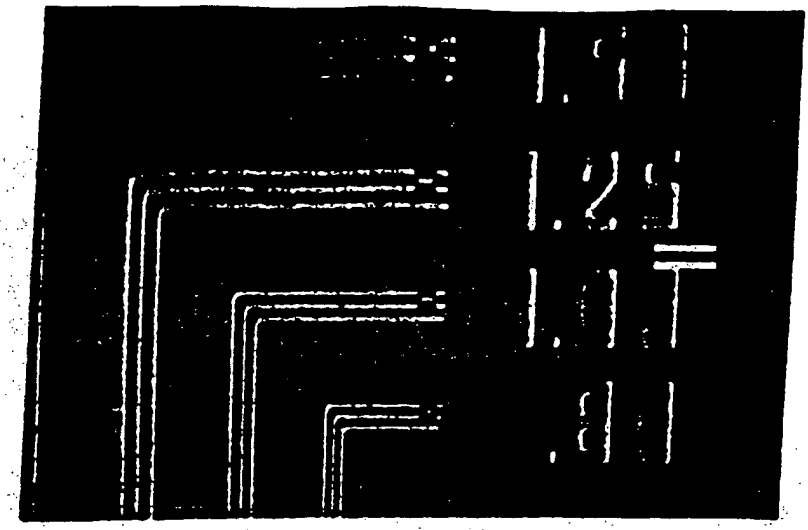
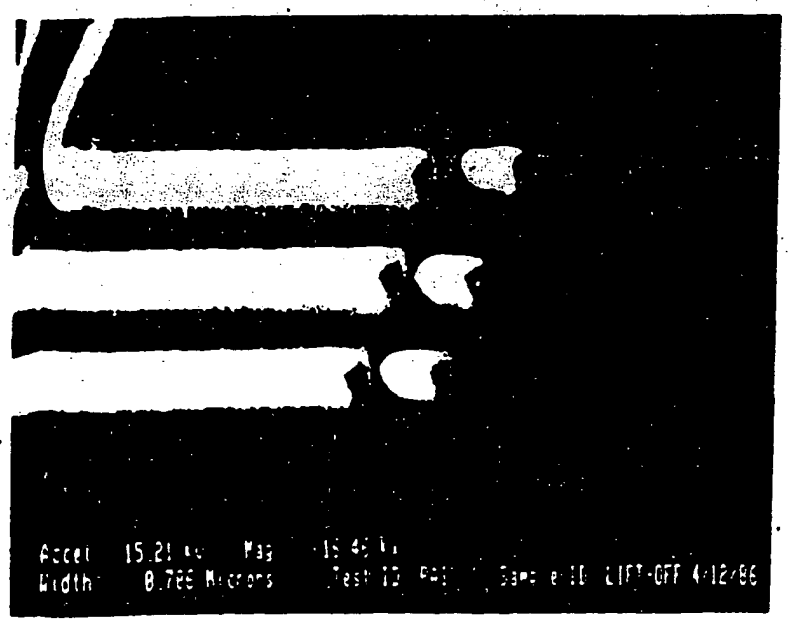


Figure 2.7: A SEM picture of 0.7 μm aluminum lines of 1μm width with 1μm space over 0.8 μm steps.

Figure 2.8: A SEM picture of 1μm Al film patterned over0.6μm steps using a tapered resist sidewalls.



(a)



(b)

Figure 2.9: A SEM picture of sub-micrometer aluminum features on a flat surface. (a) 0.8μm line and space and (b) 0.6μm line and 1.0μm space.

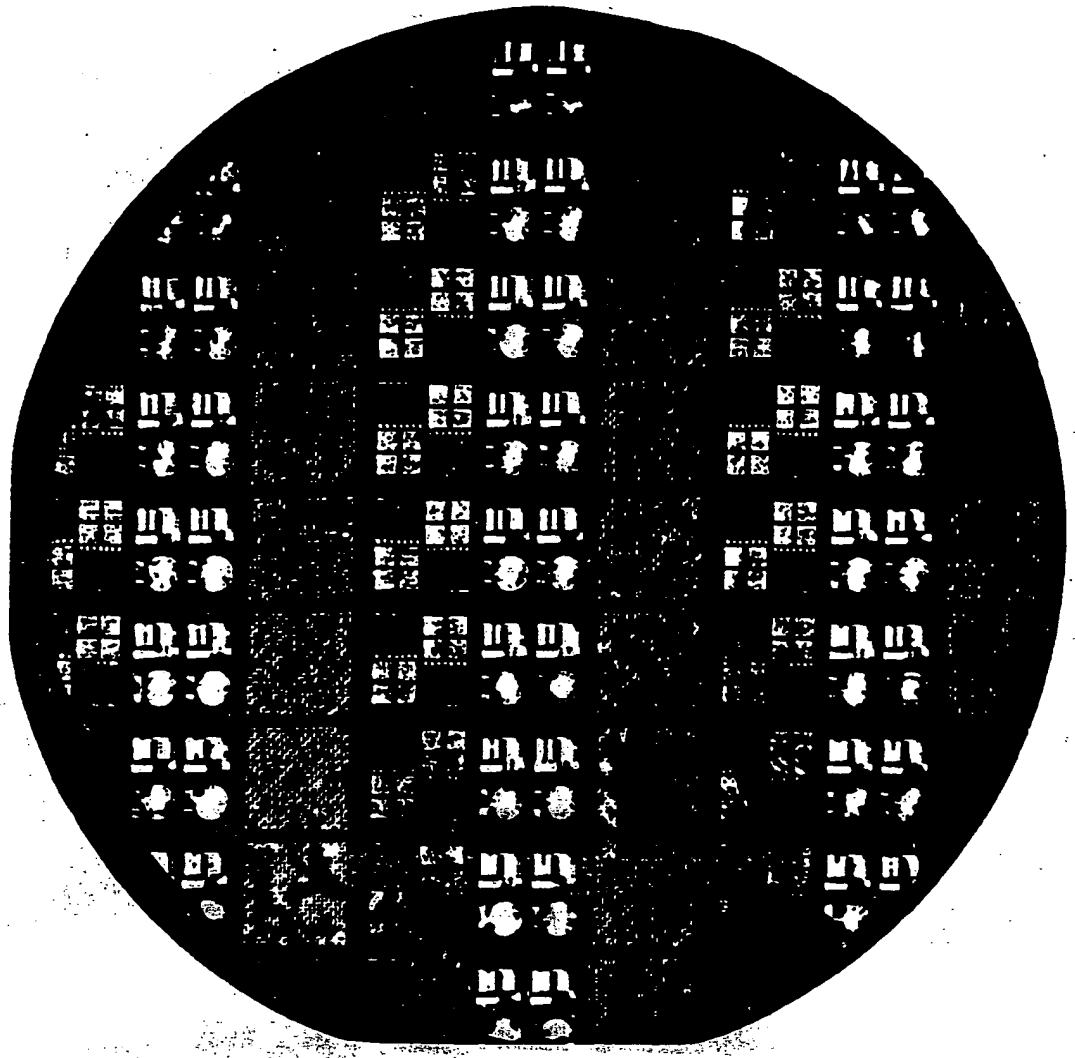


Figure 2.10: An example of the LOPED process. The dense patterns contain 0.8μm lines shown in Figure 2.9. The large squares show the ability to pattern 2.0 mm size features.

the LOPED process is limited primarily by the lithography and the metal deposition rather than the process itself.

Another application of this process is in trench isolation[5,8]. Trench patterns of 0.6μm depth are first transferred into a Si substrate by plasma etching and the resist is left in place as the lifting medium. The PHOTOX™ process is used to deposit an SiO_2 film at 100°C. A second resist layer is spun on and the LOPED etchback sequence carried out. After lift-off a planar surface is obtained, as shown in Fig.2.11.

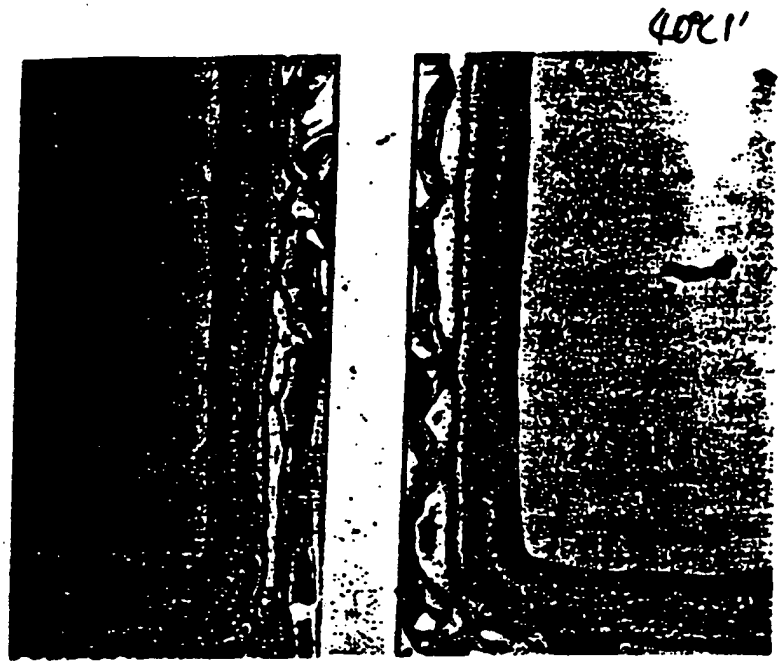
2.6 The Interaction Between Photoresist and Solvents

The interaction between the solvent and the resist has significant effects on the lifting step of the LOPED process (Fig.2.3(f)). Some solvents (e.g. acetone) swell photoresist during the process, while some other solvents (e.g. developer) simply etch photoresist. The lifting process will be examined in this section.

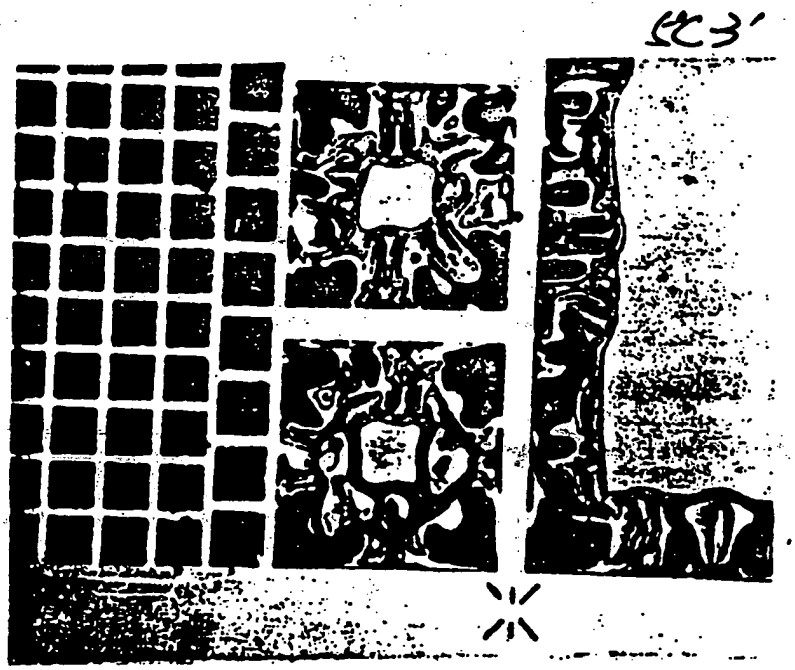
The wafers are processed as described in section 2.3 (Fig.2.3(a)-(e)). But at the last step the wafers are taken out of the solvent bath after a finite immersion time. Then the Al film is removed by wet etching. After drying, the wafers are inspected under a microscope. A sharp boundary exist between the peripheral, acetone-penetrated regions of the resist patterns and the central "un-patterned" regions (Fig.2.12). As the immersion time increases, the width of the peripheral regions increases.

The penetration depths of acetone are plotted against the immersion time in Fig. 2.13 for various metal deposition times. For each deposition time, the penetration depth increases linearly with time, or at a constant penetration velocity. As the metal deposition time increases from 2 minutes to 5 minutes, the penetration velocity decreases from 350μm/min. to 100μm/min. This decrease in the penetration velocities can be due to either a thicker film or resist cross-linking during the longer sputtering time. Another experiment has been conducted to separate the effects from these two factors. Two deposition processes are used to deposit 1μm thick aluminum films. In one experiment, a single deposition of 5 minutes is used, and in

Figure.2.11: A trench isolation example using the LOPED process. The surface is nearly flat after filling the trenches by PHOTOX™. The oxide-Si boundary, not visible in the SEM, is indicated by the white dots.



(a)



(b)

Figure 2.12: The sharp boundaries between the reacted resist regions and the unreacted core regions after a immersion in acetone bath (a) at 40°C for 1 minute and (b) at 5°C for 3 minutes.

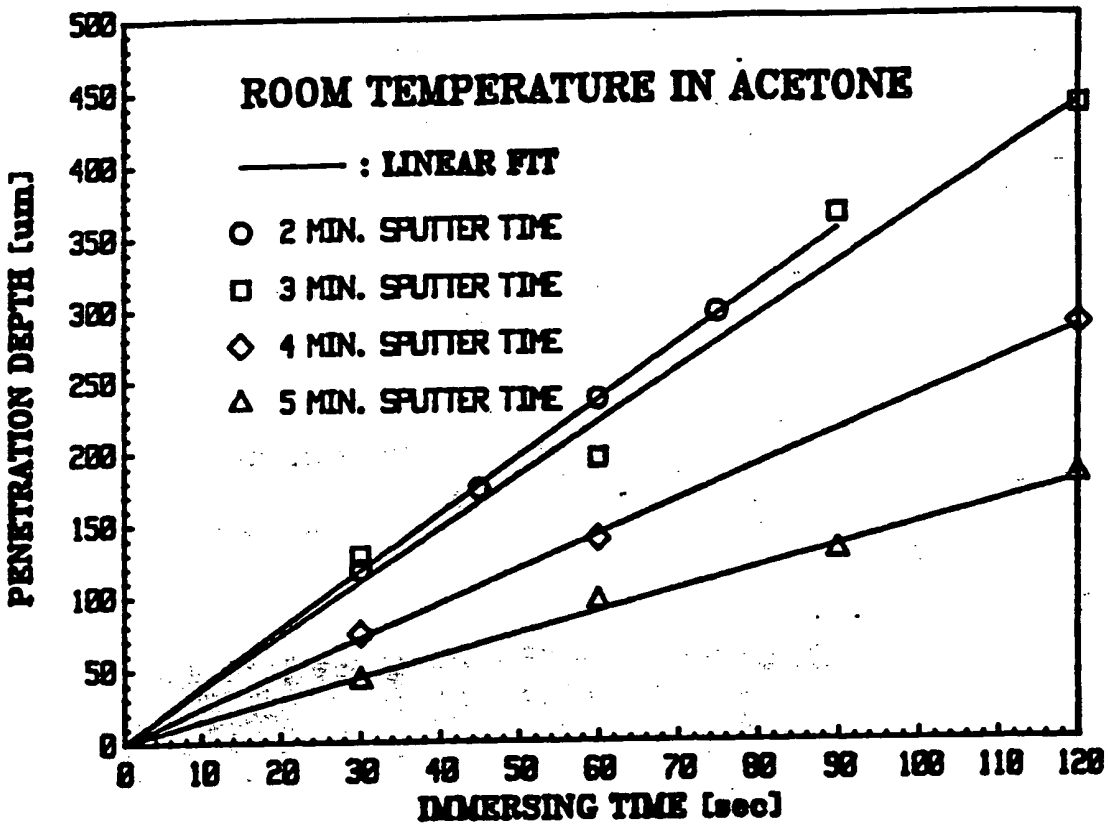


Figure 2.13: The penetration velocities of the sharp boundaries in Figure 2.11 at room temperature. The metal deposition rate is about 0.2μm/min.

the other the wafer is taken out of the vacuum chamber after a 0.5μm Al film is deposited (2 minutes and 30 seconds), followed by another deposition to complete the 1μm film. The penetration behaviors are illustrated in Fig. 2.14. The single deposition results in a much lower penetration speed than the two-step deposition, even the total thickness of the metal film is identical. Also shown in this figure is a sample with 5-minute deposition time, but half of the metal film is removed. The penetration velocity is identical to that of the thick 5-minute deposition time sample. It is then concluded that the temperature rise during the deposition process, rather than the metal film thickness, is detrimental to the penetration. The next section will examine the penetration phenomena in more detail.

2.6.1 Theoretical Analysis

The behaviour of swelling penetrants in glassy polymers has been studied extensively by polymer chemists, and it is well-known that the sorption is non-Fickian over a range of temperature and of solvent activity [24-29]. Within this range the weight gain during sorption is proportional to the first power of time (called "Case II" transport) rather than to its square root (Fickian behaviour). It is also known that a sharp boundary exists between the outer shell containing an appreciable amount of solvent and the internal core which is essentially unpenetrated.

Several models have been proposed to describe this "anomalous" behaviour. Perhaps the most satisfactory interpretation of the Case II diffusion is that of Sarti *et al.* In his model, Sarti stated that the buildup of solvent on the swollen gel side leads to a high tensile stress, which effectively pulls the polymer matrix open microscopically to permit further solvent migration. The rate of this interface migration is postulated to obey the linear law:

$$\dot{X} = K[\sigma - \sigma_c] \qquad (14)$$

where $\dot{X}$ is the rate of change of the current location of the boundary, σ is the stress, σ_c is a threshold stress and K is the proportionality constant. When the stress is lower than the threshold value, no movement is possible. At the moving boundary, the glassy core undergoes an

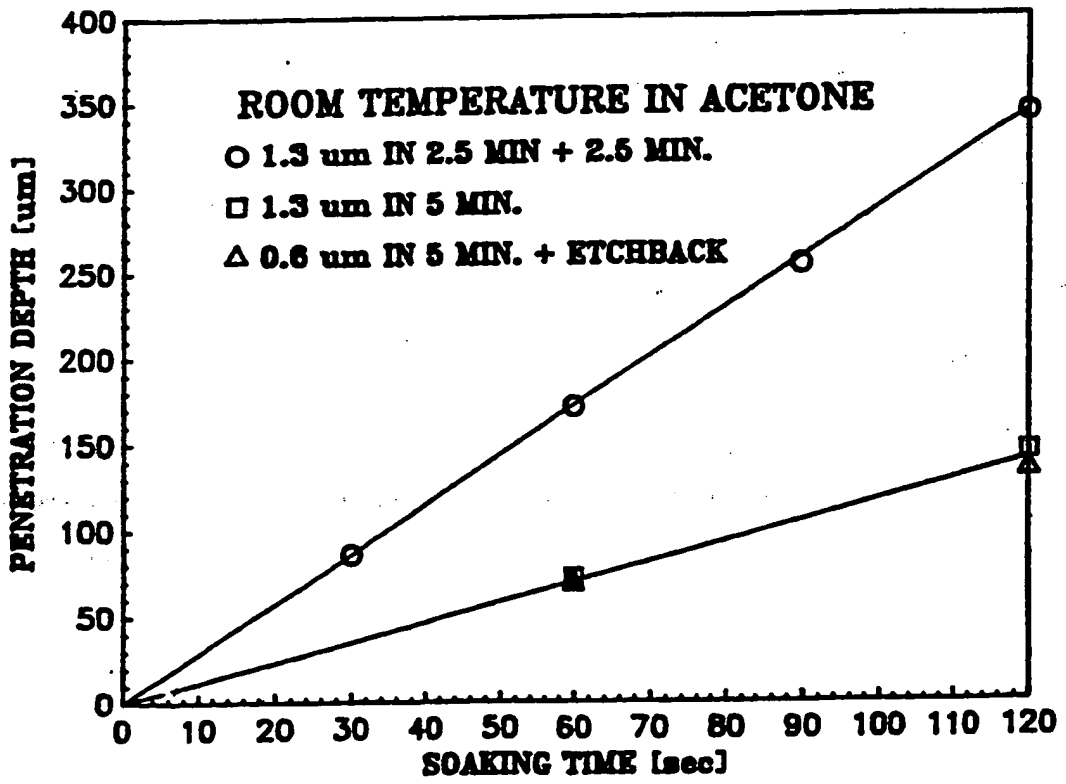


Figure 2.14: The effect of deposition time. The same deposition time (5 minutes) results in identical penetration velocities even the metal film thickness is reduced by 50%. A two-step deposition leads to faster penetration velocity for the same 1.3μm film.

osmotic stress tension π and a differential swelling stress σ_y^G[29]. Substitution of σ by ($a\pi + a'\sigma_y^G$) in equation (14), we have:

$$\dot{X} = K\,[a\pi + a'\sigma_y^G - \sigma_e] \tag{15}$$

The constants a and a' account for the fact that the osmotic tension π is isotropic, the swelling stress σ_y^G is biaxial while σ_e is uniaxial tension.

The osmotic stress can be computed by the Flory-Huggins[25] as

$$\pi = \frac{RT}{V_1}[\phi - \chi_1\phi^2 - \frac{V_1}{V_2}\ln(1-\phi)] + \pi' \tag{16}$$

where R is the ideal gas constant, T is the system temperature, V_1 is the solvent molar volume, ϕ is the solvent volume fraction in the swollen region at the boundary, V_2 is the polymer molar volume and χ_1 the Flory-Huggins parameter. π' in equation (16) represents the deviation from the equilibrium condition. If equation (16) is put into equation (15), the moving rate of the boundary is:

$$\begin{aligned} v &= \dot{X} \\ &= K(a\pi + a'\sigma_y^G - \sigma_e) \\ &= v_1[\phi - \chi_1\phi^2 - \frac{V_1}{V_2}\ln(1-\phi)] + v_0 \end{aligned} \tag{17}$$

$$v_1 = \frac{KRTa}{V_1}\ , \text{ and } v_0 = K[a\pi' + a'\sigma_y^G - \sigma_e]$$

The molar volume of acetone is 73.4 cm^3 ($=V_1$) and that of the photoresist is in the range of 4000 cm^3 to 16000 cm^3 ($= V_2$). The ratio V_1/V_2 is then negligible ($0.005 < V_1/V_2 < 0.018$) compared to other terms. The simplified equation for the penetration velocity is:

$$v = v_1(\phi - \chi_1\phi^2) + v_0 \tag{18}$$

The Flory-Huggins parameter χ_1 is given by Blank and Prausnitz[25,30]:

$$\chi_1 = 0.34 + \frac{V_1}{RT}(\delta_1 - \delta_2)^2$$

$$= 0.34 + 0.123(\delta_1 - \delta_2)^2 \tag{19}$$

The value 0.34 stands for the average value of the entropic contribution. The solubility parameter for acetone is 9.9 $(cal/c.c.)^{\frac{1}{2}}$ (δ_1) and that for novolac resin is in the range of 8.5 to 9.9 $(cal/c.c.)^{\frac{1}{2}}$ (δ_2). If these numbers are put into the equation, we have the range for χ_1 as

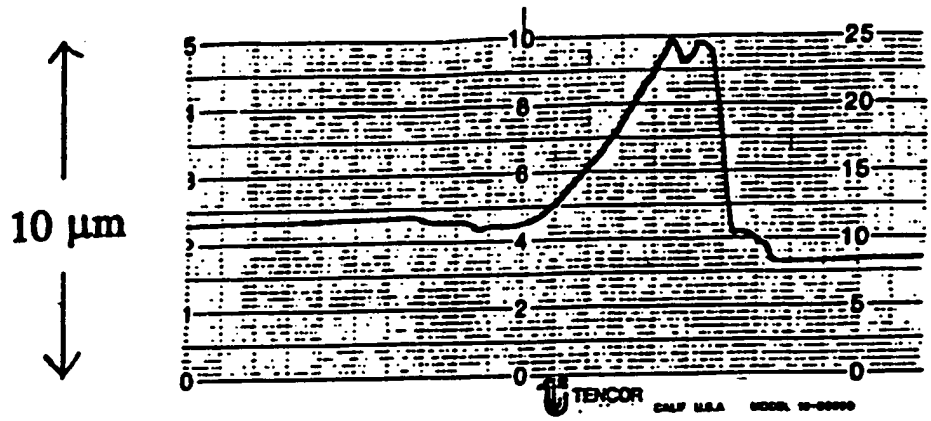
$$0.34 < \chi_1 < 0.58 \tag{20}$$

The volume fraction ϕ can be calculated from the ratio of the thickness of the swollen resist (Z_1) to that of the original resist (Z_0):

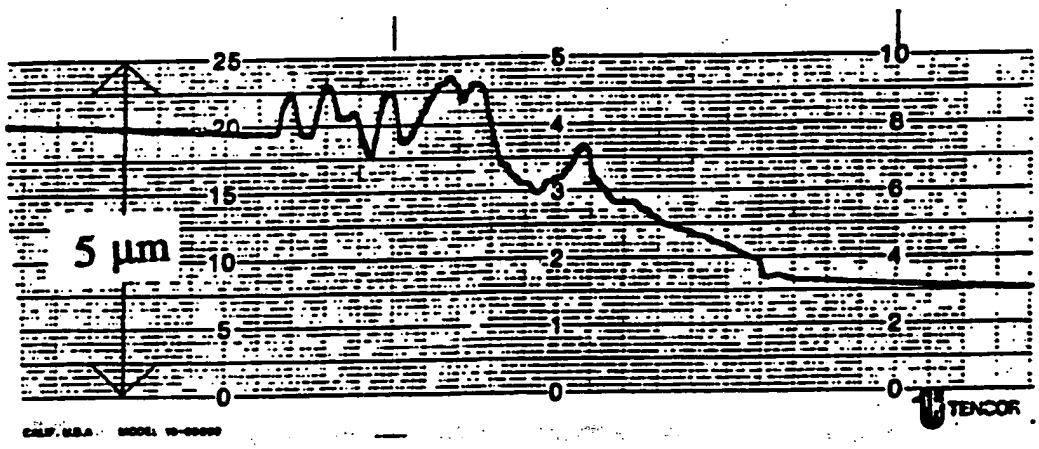
$$\begin{aligned} \phi &= \frac{Z_1 - Z_0}{Z_1} \\ &= 1 - \frac{Z_0}{Z_1} \\ &= 1 - \frac{1}{\gamma} \end{aligned} \tag{21}$$

$$\gamma = \frac{Z_1}{Z_0} \tag{22}$$

The thickness of the peripheral region is measured by a Tenco alphastep profilometer after drying the wafers (Fig.2.15), because the resist is too soft for measurement directly from the solvent bath. After drying, most of the peripheral regions collapse and result in low thickness. Part of the regions can remain the original thickness after drying, and therefore the maximum thickness recorded for each experiment is taken as the thickness of the peripheral region. For those samples with thin metal film deposited, the thickness of the resist can increase from the original 1.7μm to near 6.6μm after immersion in acetone. For the sample exposed to a longer metal deposition process, the resist swells significantly less (e.g. to 2.6μm) for the 5-minute sample. The γ values, the ϕ values as well as the corresponding penetration velocities (V) are listed in table 2.1.



(a)



(b)

Figure 2.15: The thickness of the reacted resist after drying. The metal deposition time is (a) 2 minutes and (b) 5 minutes.

Table 2.1 The Thickness Ratio (γ), Volume Fraction (ϕ) and The Penetration Velocity (V)

No.	$t_{dep.}$	γ	ϕ	V (μm/sec.)	ϕ-0.34ϕ^2	ϕ-0.58ϕ^2
1	2 min	3.88	0.742	3.97	0.555	0.423
2	3 min	2.06	0.514	3.66	0.424	0.361
3	4 min	1.71	0.414	2.37	0.356	0.315
4	5 min	1.53	0.349	1.49	0.308	0.278

The penetration velocities are plotted against $\phi - \chi_1\phi^2$ in Fig.2.16 for χ_1=0.34 and χ_1=0.58. The velocities in both curves increase linearly with $\phi - \chi_1\phi^2$ as predicted in equation (17) until a saturation velocity (= 3.97μm/min.) is reached. The fact that the penetration velocity for the least-crosslinked resist deviates from the linear dependence indicates that a mechanism other than the Case II diffusion dominates the reaction. The interface reaction rate is possibly the best explanation for the linear time dependence for the least-crosslinked sample.

2.6.2 External Effects

The lift-off process is usually improved by raising the temperature of the acetone bath or applying an ultrasonic agitation. The effects of both processes on the lifting step are investigated here. The penetration depth is plotted against the immersion time for different bath temperatures in Fig.2.17(a). The penetration velocity increases with the bath temperature. The Arrhenius plot for the penetration velocities is given in Fig.2.17(b). The activation energy is calculated to be 0.3eV.

The penetration velocity is also measured with and without the ultrasonic agitation (Fig.2.18). The addition of the ultrasonic agitation does not increase the reaction speed. Another experiment is conducted to study the effects of the agitation on the removal process. A pattern with one thousand 50μm by 50μm squares is processed by the edge detection method. After immersion in the acetone bath with ultrasonic agitation, the numbers of remaining squares are plotted in Fig.2.19 against the immersion time. If the experiment is done without the ultrasonic agitation, more than 80% of the squares (compared to 1.6% in Fig.2.19) are left

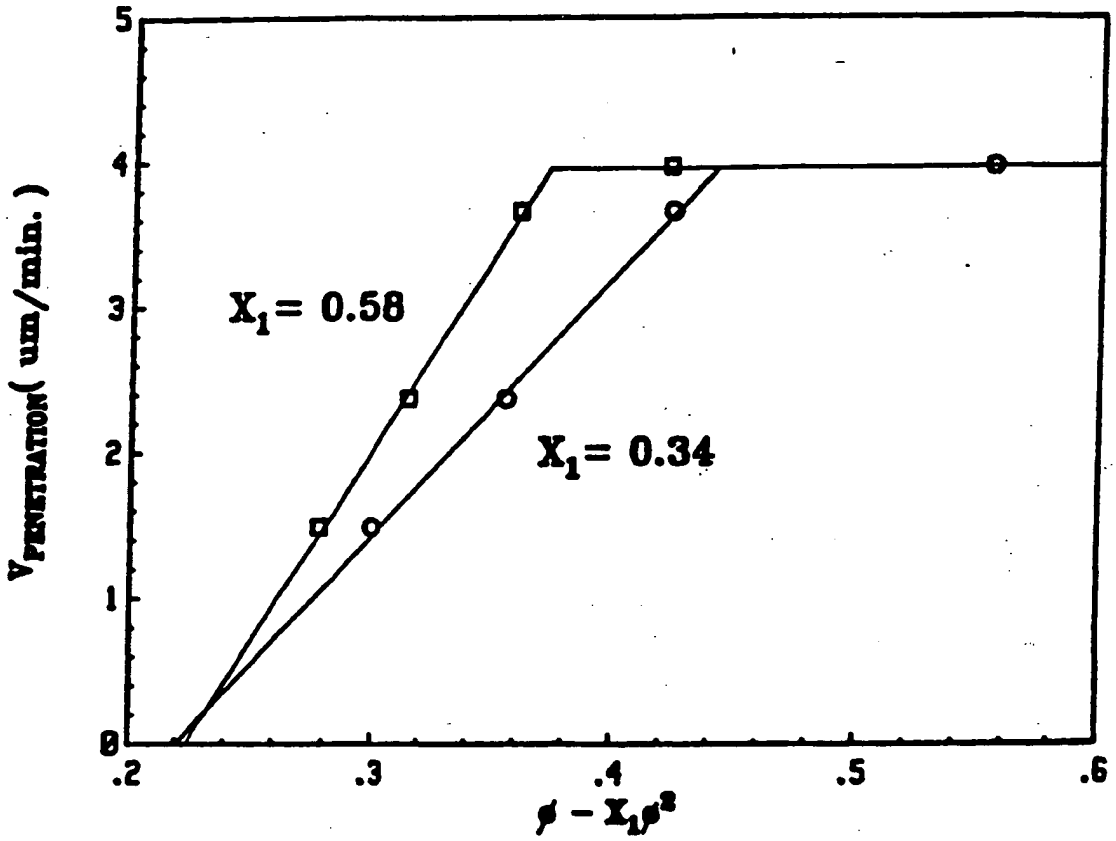
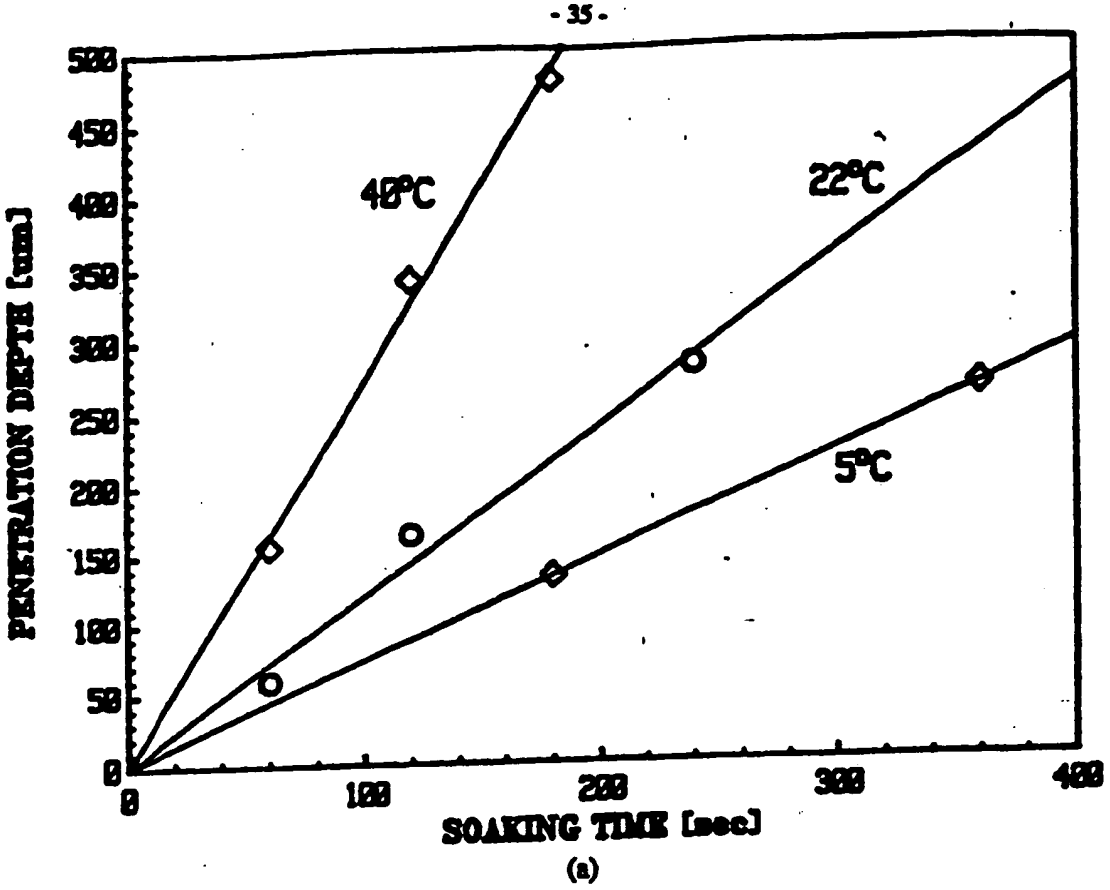
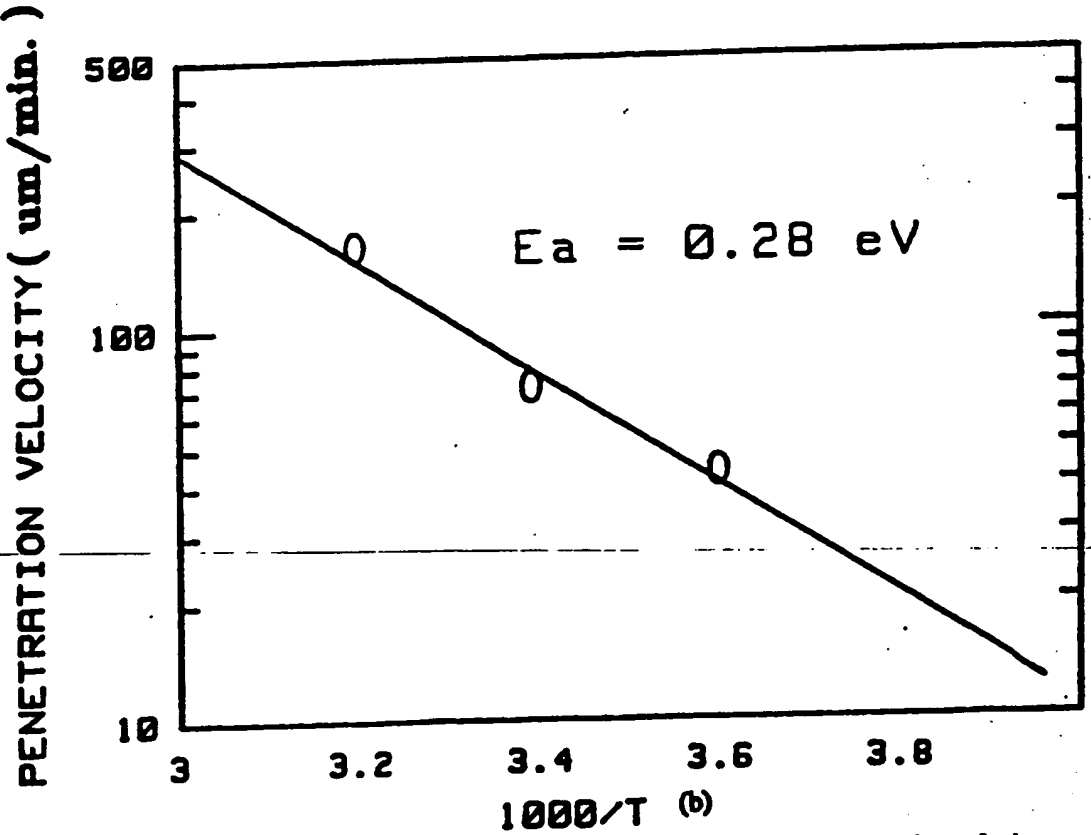


Figure 2.16: The penetration velocities is plotted versus ϕ - $\chi_1\phi^2$ for two χ_1 values, 0.34 and 0.58.



(a)



(b)

Figure 2.17: The temperature effect on the penetration velocities. (a) The penetration velocity increases with temperature. (b) The Arrhenius plot indicates an activation energy of 0.3eV.

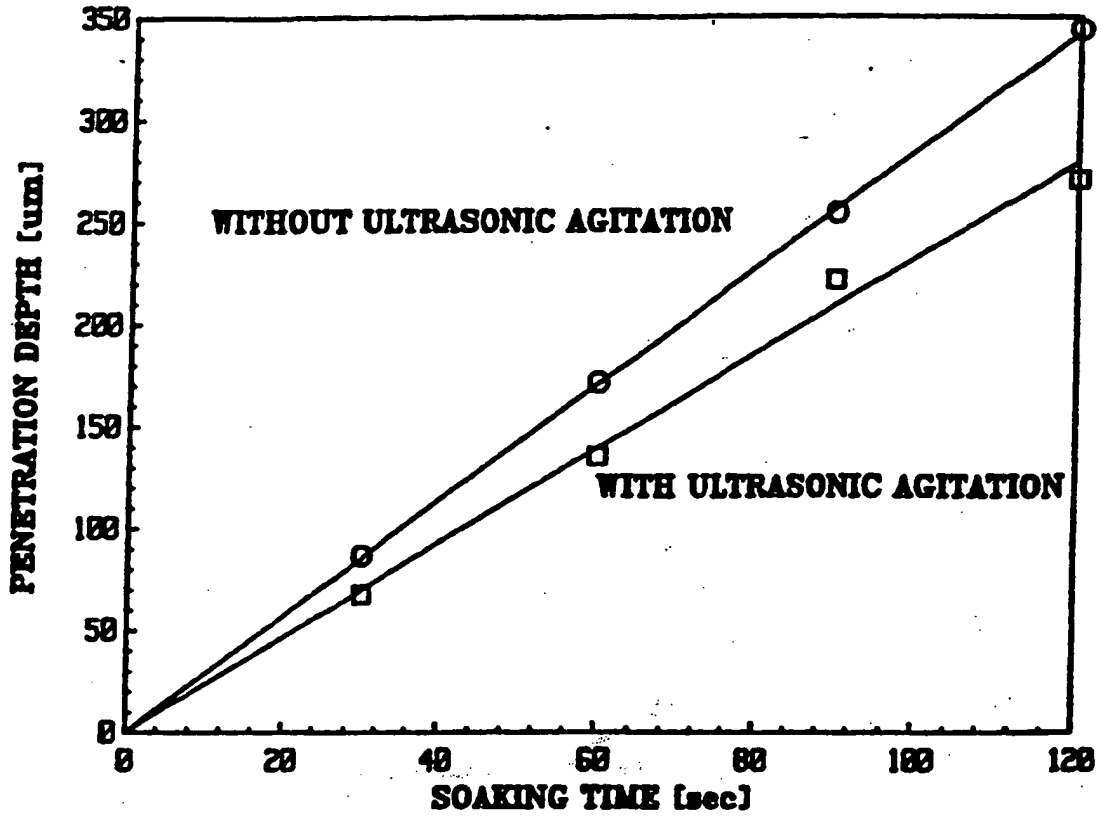


Figure 2.18: The effect of ultrasonic agitation on the penetration. The ultrasonic agitation shows no effect on the penetration velocity.

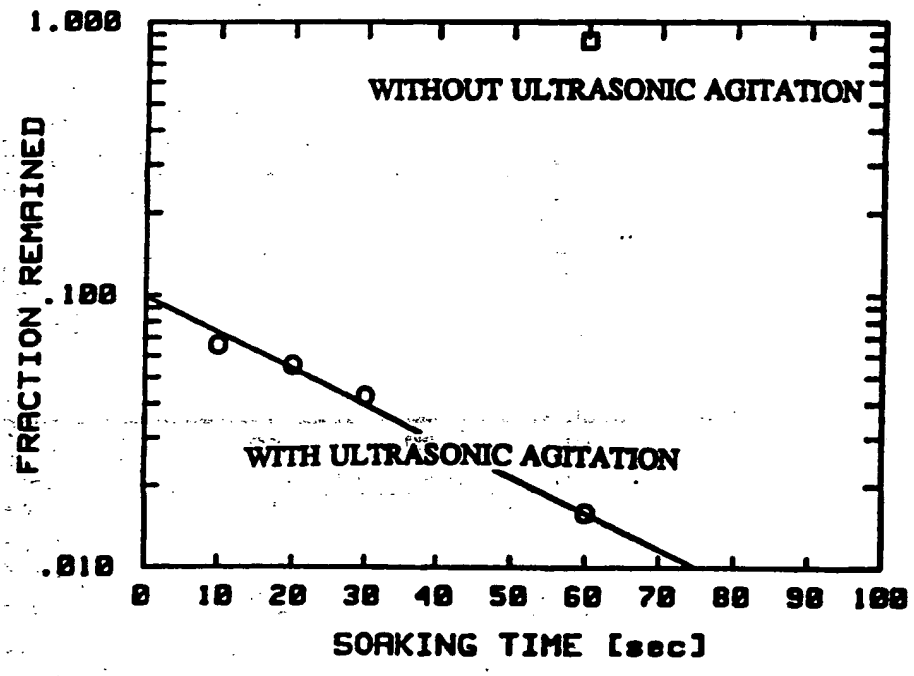
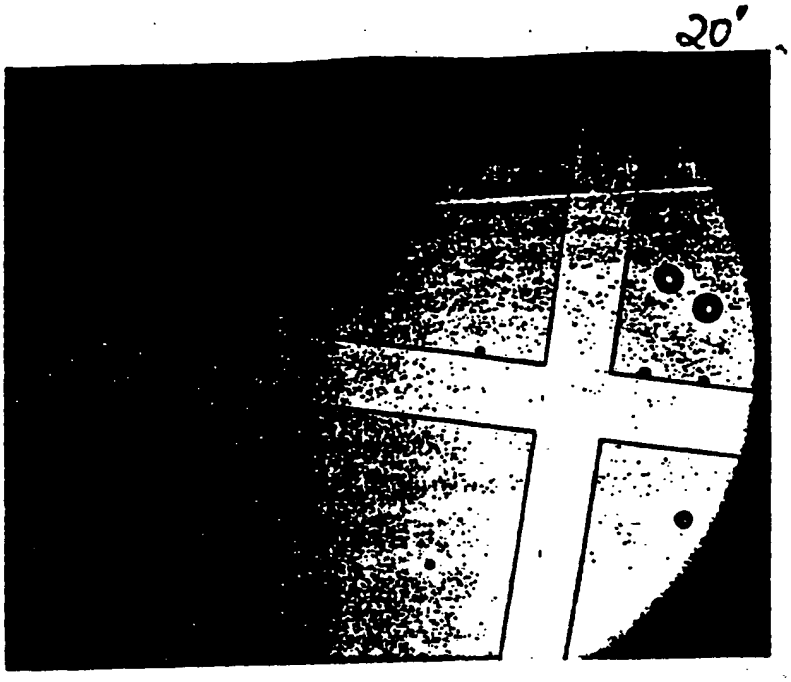


Figure 2.19: The effect of ultrasonic agitation on the lifting. The remaining resist patterns of 50μm by 50μm squares after immersion in acetone bath with ultrasonic agitation decreases exponentially with the immersion time.

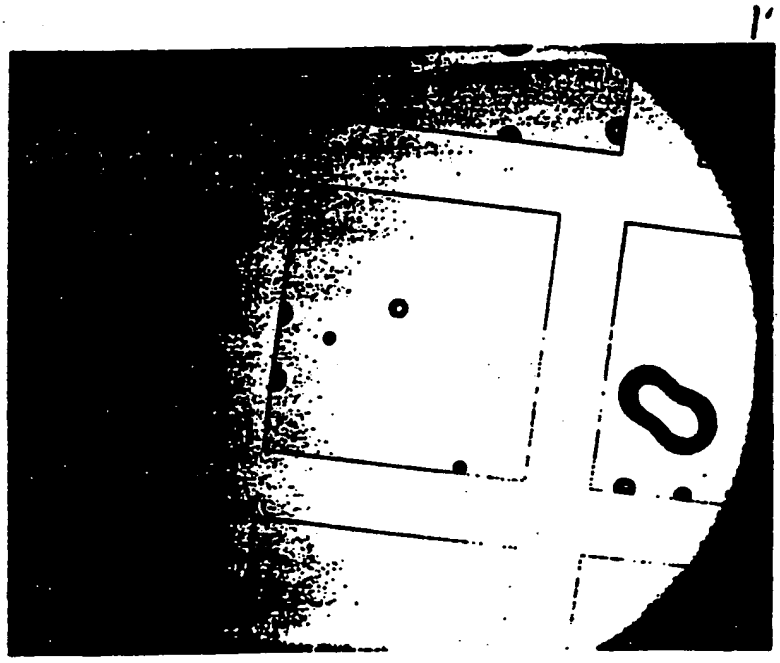
on the wafer after one minute immersion. The ultrasonic agitation apparently helps in the removal of the excess film after the underlying resist is completely penetrated by acetone. The exponential time-dependence of the remaining fraction on time ($\delta_t = \delta_0 e^{-kt}$) suggests a Poisson process, which is unique in its memoryless feature. At any time in a Poisson process, what happens after is independent of what has happened before. It is speculated that the cavitation force resulting from the ultrasonic agitation provides the external force needed to tear apart the swollen resist and remove the excess film.

2.7 Failure Mechanism for Traditional Lift-Off

All the studies discussed in previous sections deal with the lifting process with an opening to the underlying photoresist. It is also interesting to examine the lifting step when the patterning resist is completely covered by the deposited film, a case sometimes encountered with the traditional lift-off and considered "failed". For a real-time observation, the glass wafers are used as the substrate. A layer of photoresist is patterned and an Al-Si film is sputtered-deposited on the wafer. The glass wafers are placed facing downward in a petridish, with some glass slides under the edge to support the glass wafers. The setup is placed under a microscope with a 35mm camera. Acetone is poured into the petridish and pictures are taken at a fixed time interval. Some examples are shown in Fig.2.20. Whenever acetone penetrates into the resist, the Al film is locally deformed and scatters the illuminating light, resulting in an area significantly different from other areas. As the immersion time increases, the penetrated areas increase linearly with the square root of the immersion time (Fig.2.21). This penetration results in a swollen resist and tensile stress in the Al film. When the stress exceeds the tensile strength of Al, the film breaks into fragments, and any external force can remove the excess Al fragments . The lift-off process for this condition may be summarized as follows: at the beginning, acetone penetrates through the defects or pinholes of the deposited metal film into the photoresist; as the immersion time increases, more acetone diffuses into the resist and swells the resist to create a tensile stress in the metal film; when this stress exceeds the tensile strength of the deposited metal film, the film breaks into fragments; then an external force can



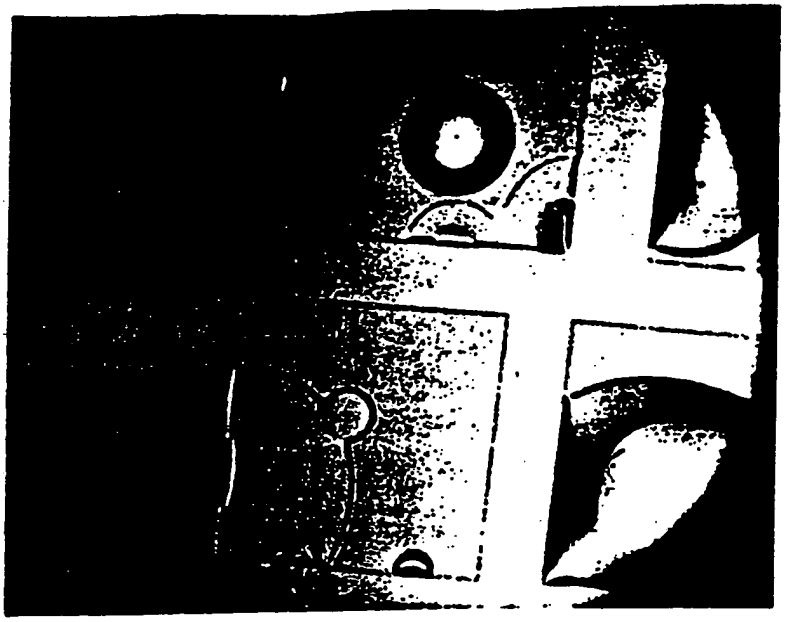
(a)



(b)

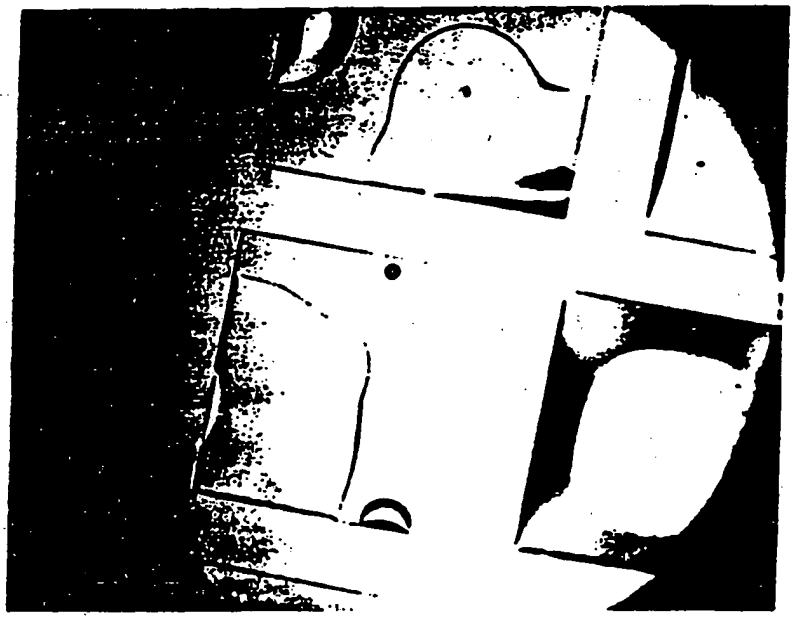
Figure 2.20: The lifting of the traditional lift-off process. The solvent penetrates through the defects of the deposited film into the underlying resist after (a) 20 seconds, (b) 60 seconds, (c) 6 minutes, and (d) 10 minutes. The reacted regions increase with the immersion time.

6'



(c)

10'



(d)

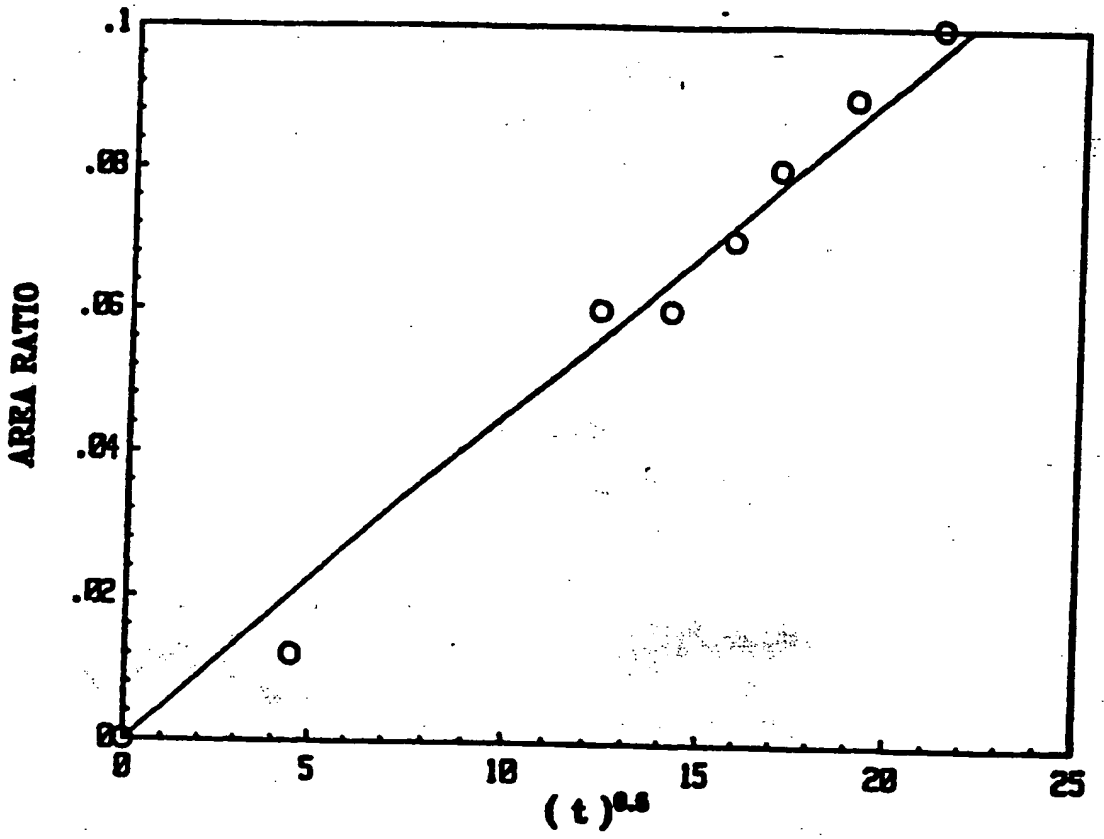


Figure 2.21: The areas of the reacted regions is plotted against the immersion time in the traditional lift-off process. A Fickian diffusion limited process shows the typical square root time dependence.

tear apart the soft, swollen resist and remove the film fragments.

This lifting step proceeds in an uncontrolled manner, and leads to unreliable results. For a large metal patterns or a thick metal film, the sidewalls of the patterning resist are easily covered even a directional deposition method (e.g. evaporation) is used for metal films. The LOPED process can circumvent this problem by providing a controlled way to create uncovered resist edges.

2.8 Why Acetone?

Several solvents have been tested for the lifting process. Acetone is a common solvent for traditional lift-off. Both the alkaline developer (e.g. AZ351) and the metal ion free developer (e.g. KTI 932) are tested. Some of the developers come as a concentrated solution from the supplier, then various concentrations are tested. Also tested are some proprietary resist strippers such as EMT-130, RT-2 and PRS-1000. The tested results are listed in table 2.2. Acetone lifts all the excess film consistently for most experiments. When heated at 80°C, the EMT-130 resist stripper (NMP as the main ingredient) etches photoresist with proportion to the square root of time. EMT-130 can remove the first few hundred micrometers of photoresist at a similar rate of acetone, but a resist pattern more than 500μm, such as the scribe line areas, requires more than 10 minutes immersion time in EMT-130 and residues can usually be observed in these areas. The concentrated developer (AZ 351) is a strong base solution, and consequently, attacks the deposited Al films. All other solutions give slow penetration velocities and incomplete lift-off. Only the small patterns on the wafers are cleared by these solvents, and an extended immersion time is always needed to lift the excess film on a large resist pattern. To lift a 200μm square resist pattern takes more than 10 minutes of the immersion for the diluted developer or the resist strippers. The same pattern can be cleared in about one minute in acetone. As a result of the slow reaction, residues of the excess films are left on the wafers. Acetone seems to be a good solvent for the lift-off. In order to understand the uniqueness of acetone, both thermodynamics and kinetics considerations have been taken.

Table 2.2 Solvents Tested for Lift-Off

Solvent	Penetration Velocity (μm/min.)	Comment
Acetone	100-350	No residues
EMT-130 (80°C)	$[170 \times (t)^{0.5}$ μm]	residues in large areas
MIBK	25	slow & residues
AZ 351 developer	-	Etch Al
AZ developer	8-10	slow & residues
MF-312	12	slow & residues
RT-2 stripper	12	slow & residues
PRS1000 stripper	20	slow & residues

The molecules in a polymer, as well as in a solvent, are attracted by other molecules of the same material. The energy per unit volume due to this attraction force is called the "cohesive energy density". A noncrystalline polymer will dissolve in a solvent of similar cohesive energy density without any further intermolecular force. If the cohesive energy density of the polymer is larger than that of the solvent, it is thermodynamically unfavored for the solvent to penetrate into the polymer and separate the polymer molecules. However if the solvent has a higher cohesive energy density it is also unlikely that the polymer molecules can dissolve into the solvent. The mathematical derivation of the aforementioned idea is presented in the following.

The process of dissolving a polymer in a solvent is governed by the free energy equation:

$$\Delta F = \Delta H - T\Delta S \tag{24}$$

Where ΔF is the change in free energy, ΔH the heat of mixing, T the absolute temperature and ΔS the entropy of mixing. The increase of entropy of dissolving a polymer in a solvent is generally quite small. Therefore the magnitude of the heat term (ΔH) is the deciding factor in determining the sign of the free energy change. A small ΔH leads to a thermodynamically

favored reaction. Hildebrand[31] proposed the most useful model for the heat term:

$$\Delta H = K[\delta_1 - \delta_2]^2 \tag{25}$$

$$\delta_1 = (\Delta E_1/V)^{\frac{1}{2}} \tag{26}$$

$$\delta_2 = (\Delta E_2/V)^{\frac{1}{2}} \tag{26'}$$

K is the proportionality factor equal to the multiple of the volume of the mixture and the volume fractions of both components. ($\Delta E/V$) is the energy of evaporation per unit volume, and is generally called the " internal pressure " or the " cohesive energy density ". The square root of the cohesive energy density, designated as δ, is called the solubility parameter. The unit of δ's is $(\text{energy/volume})^{\frac{1}{2}}$ and most values used later are in $(\text{cal/c.c.})^{\frac{1}{2}}$. As can be seen from the above equation, the minimum ΔH value is zero when δ_1 equals δ_2. The solubility parameters of some commonly used solvents are listed in table 2.3. For most commercially available photoresist, the main component is a novolac resin. The solubility parameter of the novolac resin is in the range between 8.5 to 9.9. It is clear from the table that acetone is one of the solvents that have similar solubility parameters to the novolac resin. For those water-based solvents, such as developer, the high value of the solubility parameter for water makes the dissolution of polymer thermodynamically unfavored. This is part of the reason why acetone has a relatively faster reaction. The other reason has to do with the kinetics of the reaction, or the mobility of the moving solvent molecules.

Among all the solvents with comparable solubility parameters to that of the novolac resin, acetone (CH_3COCH_3) has the smallest molecular size. As a result, the reaction kinetics, which is proportional to the mobility of the reactant, is much faster for acetone than other solvents. From both the thermodynamics and the kinetics consideration, acetone is the most favored solvent for the dissolution of novolac resin. Consequently acetone has been used as the main solvent for the lifting step.

Table 2.3 The Solubility Parameters for Some Solvents

Solvent	Solubility Parameter	Molar Volume (cm^3/mole)
MIBK	8.4	-
Xylene	8.8	178.6
Benzene	9.2	88.9
Acetone	9.9	73.4
IPA	11.5	-
Ethyl alcohol	12.7	-
Water	23.4	-

2.9 Summary

A new lift-off process using edge-detection (LOPED) has been studied as an alternative thin film patterning process for VLSI interconnection technology. Some criteria on the thickness of the top layer resist is presented to assure that the desired metal patterns are not accidentally attacked by the edge-detection method. A process window shows +/- 10% tolerance in the etching of the top layer resist and the deposited film. A 1μm line-and-space pattern of sputtered Al-Si film over topography demonstrates the potential of the LOPED process. The fact that this process does not require the reentrant profiles for the lifting medium is demonstrated by an example of using a tapered resist sidewalls process. Two submicrometer features, as well as some millimeter size patterns, suggest that the resolution of the LOPED process is limited primarily by the lithography and the metal deposition process.

The interaction between acetone and the photoresist is also investigated. A constant penetration velocity indicates a Case II diffusion process. The penetration velocity is found to follow the $\phi - \chi_1\phi^2$ dependence as predicted by a Case II diffusion model, until a saturation velocity of 3.97μm/sec. is reached. A higher bath temperature increases the penetration velocity with an activation energy of 0.3eV. The ultrasonic agitation does not increase the penetration velocity, but rather helps in removing excess film fragments. If the underlying resist is

completely covered by the deposited metal film, the acetone can only penetrate through the metal film in an unpredictable way. Then the swollen resist introduces a tensile stress in the metal film until it breaks. An external force can remove the film fragments from the wafer to complete the process.

Acetone is found to be a good solvent for lift-off because it has a similar solubility parameter as the novolac resin and a small molecular size. Other solvents, such as developers and resist strippers, react with the photoresist in a slow way and leave residues on the wafer.

2.10 Reference

[1] T. Moriya, S. Shima, Y. Hazuki, M. Chiba, M. Kashiwaga, " A Planar Metallization Process-Its Application to Tri-Level Aluminum Interconnection," *1983 IEDM*, p.550 (1983).

[2] I. Beinglass, " Selective CVD Tungsten Deposition - A New Technology for VLSI and Beyond," *1985 Silicide Workshop*, Material Research Sco., p.13 (1985).

[3] D.W. Widmann, " Metallization of Integrated Circuits Using a Lift-Off Technique," *IEEE. J. Solid-State Circuits*, SC-11, 466(1976).

[4] M. Hatzakis, B.J. Canavello, J.M. Shaw, " Process for Obtaining Undercutting of a Photoresist to Facilitate Lift-Off," *IBM Tech. Disl. Bull.*, 19, 4048 (1977).

[5] J.S. Logan, G.C. Schwaltz, L.B. Zielinski, " SiO2 Barrier Layer Lift-Off Process," *IBM Tech. Disl. Bull.*, 20, 1024 (1977).

[6] M. Hatzakis, B.J. canavello, J.M. Shaw, " Single-Step Optical Lift-Off Process," *IBM J. Res. Develop.*, 24, 452 (1980).

[7] G.G. Collins, C.W. Halsted, " Process Control of the Chlorobenzene Single-Step Lift-Off Process with a Diazo-Type Resist," *IBM J. Res. Develop.*, 26, 596 (1980).

[8] J.H. magerlin, D.J. Webb, " Electro-Beam Resists for Lift-Off Processing with Potential application to Josephson Integrated Circuits," *IBM J. Res. Develop.*, 24, 554 (1980).

[9] L. Land, L.Merces, S. Miller, " Metal Lift-Off Techniques for Micron and Submicron Geometries," *Kodak Microelectronic Semlar, Interface '80*, 93 (1980).

[10] Y. Homma, H. Nozawa, S. Hanada, " Polyimide Lift-Off Technology for High Density LSI Metallization," *IEEE Trans. Electron Devices*, ED-28, 552 (1981).

[11] S.P. Lyman, J.L. Jackel, P.L. Liu, " Lift-Off of Thick Metal Layers Using Multilayer Resist," *J. Vac. Sci. technol.*, 19(4), 1325 (1981).

[12] T. Serikawa, T. Yachi, " Lift-Off Patterning of Sputtered SiO2 Films," *J. Electrochem. Soc.*, 128, 918 (1981).

[13] R.M. Halverson, M.W. Macintyre, W.T. Motsiff, " The Mechanism of Single-Step Lift-

Off with Chlorobenzene in a Diazo-Type Resist," *IBM J. Res. Develop.*, 26, 590 (1982).

[14] A.A. Milgram, "Lift-Off Process for Achieving Fine-Line Metallization," *J. Vac. Sci. Technol.*, B1(2), 658 (1983).

[15] K. Arai, F.Yanagawa, S. Kurosawa, " Influences of Molecular Reflection on the Lift-Off Pattern Edge Quality," *J. Vac. Sci. Technol.*, B2(4), 658 (1984).

[16] Y. Yamashita, R. Kawasa, K. Kawamura, S. Ohno, " New, Deep UV Resist (LMR) for Lift-Off Technique," *J. Vac. Sci. Technol.*, B3(1), 314 (1985).

[17] A. Fathimulla, " Single-Step Lift-Off Process Using Chlorobenzene Soak on AZ4000 Resist," *J. Vac. Sci. Technol.*, B3(1), 25 (1985).

[18] T. Yachi, T. Serikawa, " Lift-Off Patterning of Sputtered SiO2 Films (LOPAS) and Its Application to Recessed Field Isolation," *J. Electrochem. Soc.*, 132, 2775 (1985).

[19] P.L. Pai, Y. Shacham-Diamand, W.G. Oldham, "High Resolution Additive Thin Film Patterning," *Kodak Microelectronic Seminar, Interface '85*, (1985).

[20] Y. Mimura, " The Mechanism of Overhang Formation in Diazo/Novolac Photoresist Film by CHlorobenzene Soak Process," *J. Vac. Sci. Technol.*, B4(1), 15 (1986).

[21] P.L. Pai, Y. Shacham-Diamand, W.G. Oldham, "A High Resolution Lift-Off Technology for VLSI Interconnections," *VLSI Multilevel Interconnection Conf.*, (1986).

[22] P.L. Pai, W.G. Oldham, "Metallization Approaches Using Lift-off and Spin-on Glass," *the 1987 International Symposium on VLSI Technology, System and Applications*, (1987).

[23] Y. Homma, A. Yajima, S. Hanada, " Feature Size Limit of Lift-Off Metallization Technology," *IEEE Trans. Electron Devices*, ED-29, 512 (1982).

[24] D.S. Soong,"Dissolution Kinetics of E-Beam Resist," *SPIE Proceedings*, 539, 2 (1985).

[25] G.C. Sarti, " Solvent Osmotic Stress and the Prediction of Case II Transport Kinetics," *Polymer*, 20, 827 (1979).

[26] N.L. Thomas, A.H. Windle, " A Deformation Model for Case II Diffusion," *Polymer*, 613 (1980).

[27] C.M. Hansen, " Diffusion in Polymer," *Polymer Eng. and Sci.*, 20(4), 252 (1980).

[28] G.C. Srati, Apicella, " Non-Equilibrium Glassy Properties and Their Relevance in Case II Transport Kinetics," *Polymer*, 21, 1031 (1980).

[29] C. Gostoli, G.C. Srati, " Diffusion and Localized Swelling Resistances in Glassy Polymer," *Polymer Eng. and Sci.*, 22(16), 1018 (1982).

[30] R.F. Blanks, J.M. Parnsnitz, *IEC Fund*, 1964,3,1.

[31] J.H. Hildebrand, R.L. Scott, ' Solubility of Nonelectrolyte,' Reinhold, New York, 1950.

Chapter 3
A Planarization Process Using Spin-On Glass

3.1 Introduction

For multilevel interconnection technology, a planarization process is needed for better step coverage of subsequent depositions. The use of spin-on glass (SOG) is attractive because it can provide good planarity at a relatively low cost [1-8]. There are two approaches to using SOG, the etch-back process and the non-etchback process. In the etch-back process, the SOG is used as a sacrificial layer and is either completely removed or partially removed later in the process. There is no SOG left over the underlying metal patterns in the etch-back process. Conversely, the SOG in the non-etchback process is part of the interlayer dielectric film. In principle, the non-etchback process is simpler than the etch-back process. However, it is found that in the non-etchback process the buried SOG film, when exposed to the vias, may contaminate the second layer of metal and result in a high via resistance ("poisoned via"). As a result, most of the reported applications of SOG are the etch-back approaches [2-6].

In this section we explore the limit of the etch-back process first. The SAMPLE simulation program is extensively used to determine the deposition as well as the etching profiles [9]. Then a study of the non-etchback process is conducted to give some guidelines for using the process. An empirical model for the spin-coating profile of spin-on glass is proposed and is used in conjunction with the SAMPLE program to show the effectiveness of the the planarization process in improving the step coverage. In the following sections, the development of a non-etchback process is described. The material properties, as well as the roles of the annealing, are investigated. Infrared spectrophotometry is used to study the annealing effects on the contents of hydroxyl and organic groups. Both the room-temperature stress and in-situ stress during annealing are also examined. Dielectric properties (including dielectric constants, dissipation factors and breakdown fields) are studied as a function of annealing conditions.

3.1.1 The Limit of the Etch-Back Process

A typical example of the etch-back planarization process using SOG is described below. First a thick dielectric film (generally much thicker than the desired thickness of the interlayer dielectric film) is deposited over the patterned metal layer. Then the spin-on glass film is coated and annealed. A plasma etch, which can remove the SOG film at a similar rate as of the dielectric film, transfers the smooth topography of the SOG film into the dielectric film. The process is completed by another deposition of the dielectric film to achieve the required final thickness.

The requirement that all the SOG film over the underlying metal must be removed, as needed to assure the absence of the "poisoned vias", sets the process window for a specific combination of film thicknesses. For a narrow isolated metal line, the thickness of the SOG film on top is negligible compared to the SOG film thickness on a flat surface(Fig.1). Therefore, the maximum amount that can be etched before the underlying metal film is exposed and resputtered is the thickness of the deposited dielectric film:

$$\Delta H_{MAX} = H_{OX} \tag{1}$$

The condition that determines the minimum amount needed to be etched is shown in Fig.2 for a standard LOCOS-isolation, polysilicon-gate MOS process. The worst-case step, equal to the thickness of the polysilicon plus half the field oxide, "propagates" through the metal film. The following deposition of the metal film and the thick dielectric film will retain, if not increase, the step height. For a narrow gap of the dielectric film, the SOG film most likely will planarize the topography and result in a maximum thickness equal to the sum of the step height and the SOG film thickness. Consequently, the minimum amount of the etching to remove all the SOG film over metal patterns is

$$\Delta H_{MIN.} = \left(\frac{H_{FOX}}{2} + H_{\phi\text{-}Si} + t_{SOG} \right) / S \ , \tag{2}$$

where S is the selectivity of the etching, defined as the ratio of the etch rate of the SOG to that of the deposited dielectric film.

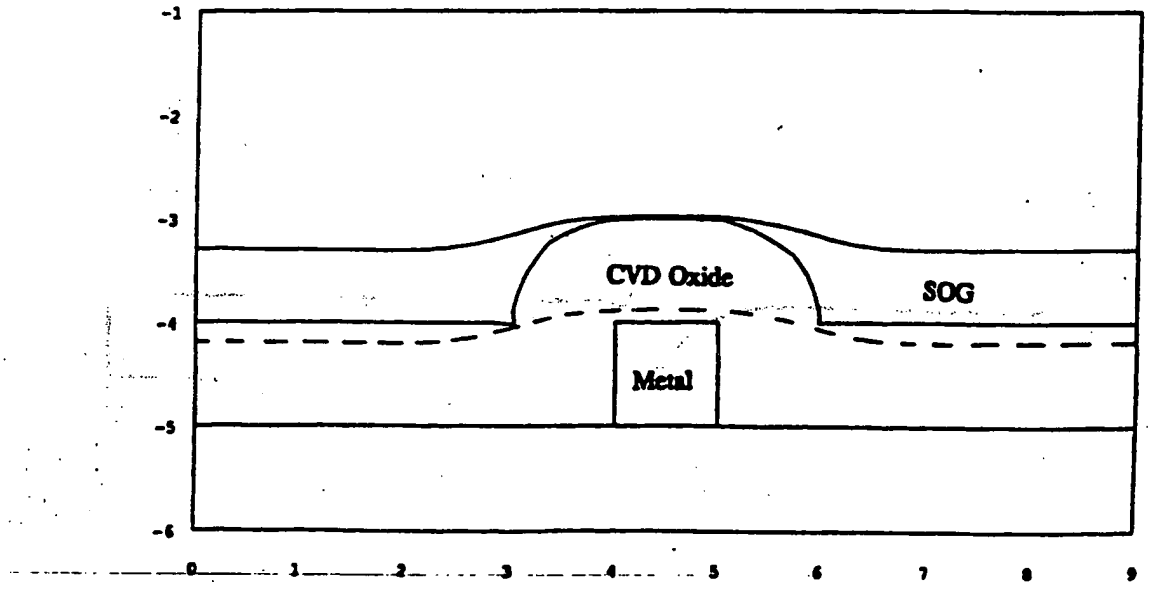


Fig.3.1 The simulation of a spin-on glass film coated over an isolated metal line.

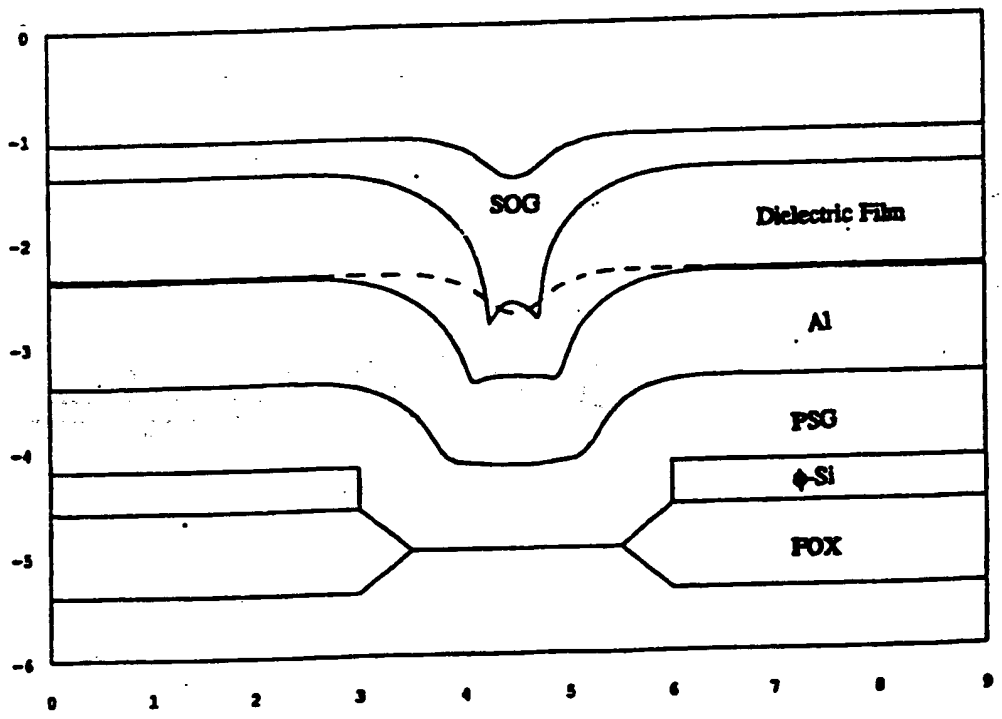


Fig.3.2 The simulation of a spin-on glass film coated over surface topography.

For a practical process, the acceptable process window must have a reasonable margin to allow for process variations and non-uniformity. It is then required that the upper limit of the etching (the maximum amount) must be larger than the lower limit (the minimum amount) by a safety margin ($\sigma\%$):

$$\Delta H_{MIN.} \times (1 + \sigma\%) < \Delta H_{MAX.} \quad (3)$$

If equation (1) and equation (2) are substituted into equation (3), we have the constraint on the dielectric film thickness for the etch-back process :

$$(\frac{H_{FOX}}{2} + H_{\phi\text{-}Si} + t_{SOG})/S \times (1 + \sigma\%) < H_{OX} \quad (4)$$

A realistic example has the following film thicknesses and process parameters: field oxide 0.6μm (H_{FOX}), polysilicon 0.4μm ($H_{\phi\text{-}Si}$), SOG film 0.2μm (t_{SOG}); the selectivity of the etching is 1.0 (S) and the safety margin is 20% (σ). Then equation (4) shows that:

$$0.98\mu m < H_{OX} \quad (5)$$

Or a minimum dielectric film thickness of about 1μm is needed.

It is obvious from equation (4) that a thicker dielectric film can allow a larger process window. But the shadowing effect of the deposition limits the maximum thickness for a given metal space. A purely isotropic deposition over a step will only reduce the space until the sidewalls merge. But the most widely used low-temperature CVD oxide (LTO) and the plasma-enhanced CVD (PECVD) oxide have some degree of directionality. For a narrow trench, the film deposited at the sidewalls and at the bottom is significantly less than that deposited on the tops. As the film thickness increases, the film on the top levels tends to merge and leaves under it a pocket with a narrow opening or a sealed void. The etch-back following after the SOG processing may open the voids or the poorly filled pocket, and thus result in severe topography for further depositions.

The SAMPLE program has been used to simulate the deposition process with varying metal spaces. The underlying metal film is chosen to be 1μm thick; a PECVD process is

simulated as the dielectric deposition method; a critical gap of 0.3μm is arbitrarily chosen as the minimum width needed for successful filling of SOG. The maximum dielectric film thickness is shown in Fig.3 for two deposition temperatures (or two surface migration ranges). From this figure, the minimum metal space of 1.2μm is needed if more than a micrometer dielectric film is needed as mentioned in the last paragraph. Any demand of a thicker dielectric film or of a smaller metal space must be met with a different process than the simple etchback process just described. One possible solution is to use a multiple-etchback process, a thinner dielectric film is repeatedly deposited and etched back until the desired planarity is acquired. Another potential solution avoids etchback entirely.

3.1.2 The Limit of a Non-Etchback Planarization Process

A non-etchback planarization process using spin-on glass is potentially much simpler than the process just described. The limitation mentioned in the last section is removed since the CVD-deposited dielectric film is much thinner in the non-etchback process. However, the "poisoned via" problem associated with the non-etchback process must be solved by selecting the right material and process parameters. The development of a non-etchback process will be discussed in the next section. In this section, we will explore the fundamental limit of the non-etchback process.

An empirical model is used to describe the coating profiles of SOG over topography. Based on the examination of cross-sections using scanning-electron microscopy, we have formulated an empirical model for the coating profile:

$$y = y_\infty + (y_0 - y_\infty)\exp[-(\frac{A}{t_0} + \frac{B}{H})x] \ , \qquad (6)$$

where A and B are two constants depending on the SOG material and process parameters only, t_0 is the SOG film thickness on a flat surface, and H is the step height. As an example, the constants for the SOG 305 from Allied Co. are A=0.44 and B=1.36.

This model is used in conjunction with the SAMPLE simulation program to study the

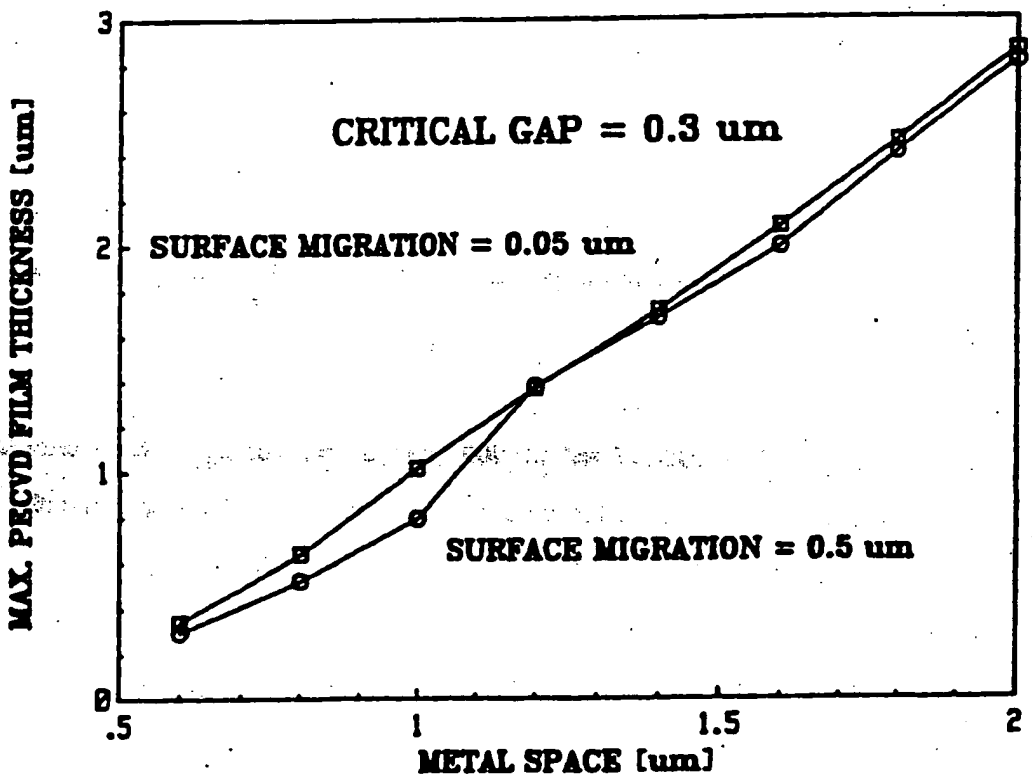


Fig.3.3 The maximum thickness of PECVD oxide before a deep pocket or a sealed void is formed. The underlying metal thickness is assumed 1μm, the SOG is assumed 200nm, and the minimum gap needed for a successful filling is 0.3μm.

effectiveness of the SOG planarization process. An isotropic deposition over an SOG-coated step is simulated and followed by a sputter-deposition of a metal film. The step coverage is defined as the ratio of the thinnest film thickness divided by the thickness on a flat surface. The simulation with a 0.2μm SOG film is repeated for various values of the space in the underlying topography (Fig. 4). As can be seen from the figure, the singly-coated SOG film is not effective in improving the step coverage. At a metal space of 1.5μm, the step coverage (20%) is about one half of the step coverage (40%) for a wide space. The simulation of the metal deposition is for an ideal (hemispherical) sputtering distribution; the actual step coverage can be worse than this. The SEM pictures in Fig.5 show the step coverage of a sputter-deposited Al-Cu-Si film from a CPA sputtering system. The step coverage over an isolated metal line is significantly improved by SOG-coating (Fig.5(a)). The step coverage for a narrow space (Fig.5(b)) is good since the dielectric film has planarized the topography. The step coverage of a wide space (Fig.5(c)) is also good since a larger incidence angle is possible on the sidewall(d At a space of about 1.5μm (Fig.5(c)), the combination of the SOG film and the deposited dielectric film create a deep trench at the center of the space. The deposition of the metal film cannot fill the trench, thus resulting in very little film on the sidewalls (" forbidden gap "). To circumvent the problem, either a thicker SOG film is needed for better planarization, or a sandwich structure of SOG/CVD Oxide/SOG must be used.

Several commercially available SOG products have been evaluated for the non-etchback process. Two SOGs (SOG-208 and IC1-200) with the best coating properties were chosen for a more detailed study. SOG-208 contains methyl, phenyl and ethoxy groups with carbon content in the range of 20-30%. IC1-200 has a similar carbon content as SOG-208 and contains only methyl and unspecified alkoxy groups bonded to silicon atoms. The solvent for SOG-208 is primarily propanol and the solvent for IC1-200 is primarily butanol. SOG-B also contains a "leveling agent" to assist in obtaining a uniform coat. Overall, the higher boiling point solvent and the added leveling agent give IC1-200 a better coating uniformity than SOG-A.

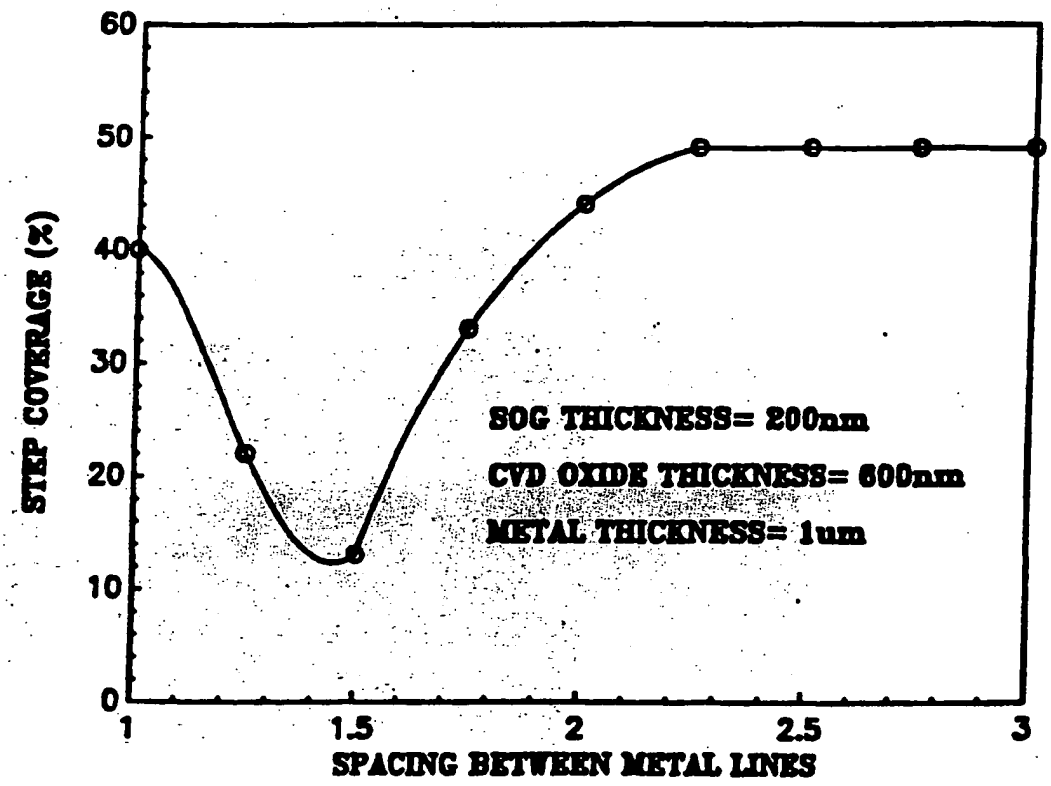
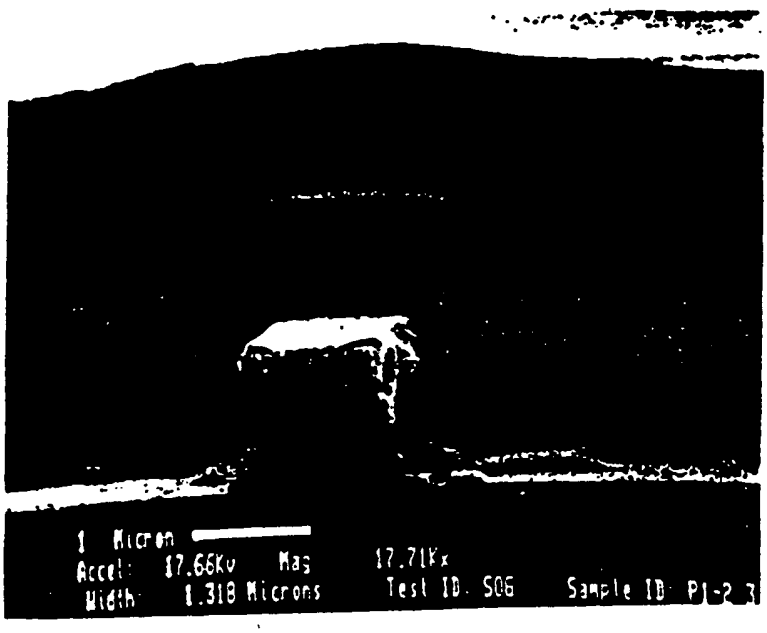
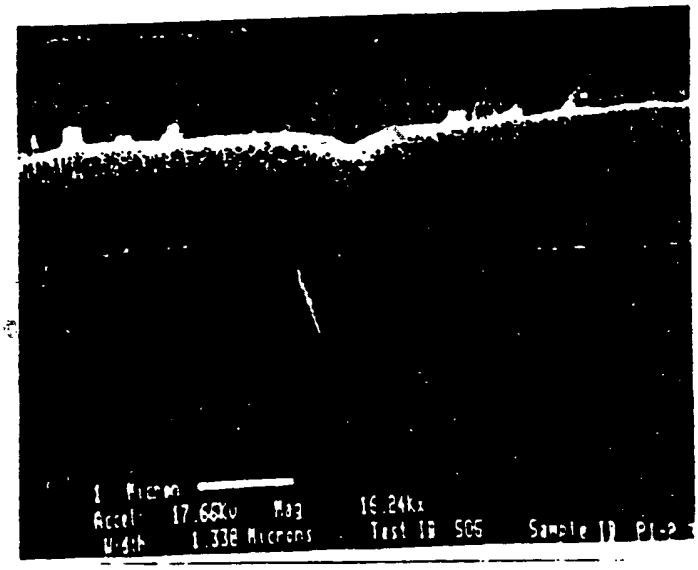


Fig.3.4 The step coverage of a hemispherical sputtering over a SOG/CVD dual layer over underlying metal topography. The underlying metal film is assumed 1μm, the SOG film is 200nm, the CVD oxide is 600nm, and the top layer metal is 1μm.

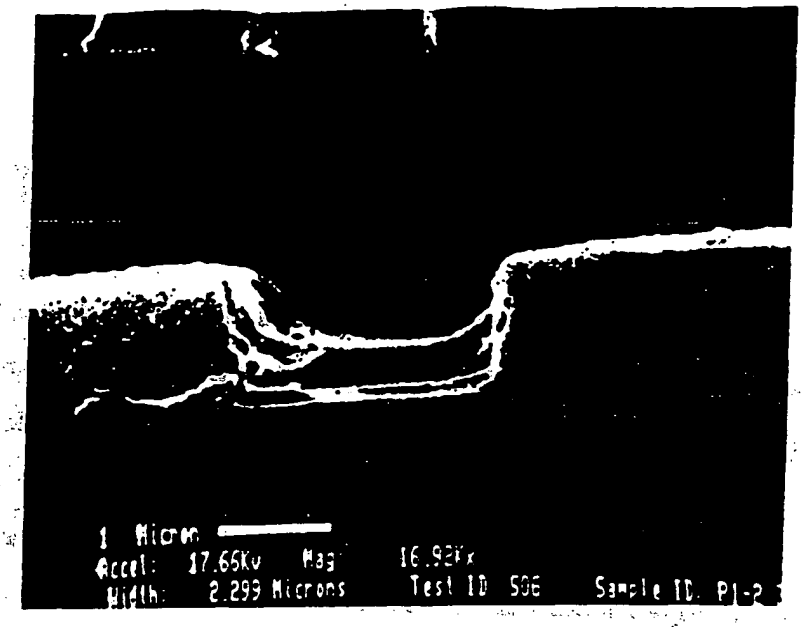


(a)

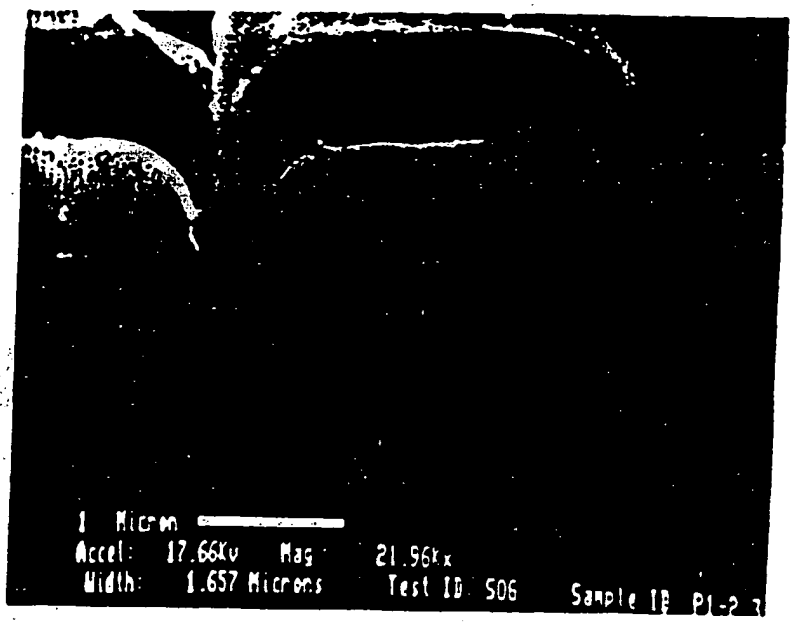


(b)

Fig.3.5 The step coverage of the sputtered metal over SOG-smoothed topography. (a) The step coverage over an isolated metal line is improved. (b) The step coverage for a 1.0μm metal space is improved by SOG. (c) The step coverage for a 2μm metal space is also improved. (d) The step coverage for a 1.5μm metal space is extremely bad due to the formation of a "forbidden gap".


1 Micron
Accel: 17.66Kv Mag 16.92Kx
Width: 2.299 Microns Test ID: S06 Sample ID: PI-2

(c)


1 Micron
Accel: 17.66Kv Mag 21.96Kx
Width: 1.657 Microns Test ID: S06 Sample ID: PI-2

(d)

3.2 Experimental Setup

3.2.1 Materials

A. Substrates

The substrates used in most of the experiments are 100mm-diameter, p-type (100) Si wafers. The resistivity of the wafers is between 5 Ω-cm to 50 Ω-cm, or equivalently the doping concentration between 2×10^{14} cm^{-3} to 2×10^{15} cm^{-3}. If a metallic electrode is needed under the SOG film, an aluminum film is sputter-deposited on the Si wafers before SOG processing. Some other experiments (e.g. surface resistance and contact resistance measurements) require a patterned conductive film under the SOG, in this case sputter-deposited Al films are patterned on oxidized Si wafers.

B. Spin-on Glass (SOG)

Table 3.1 SOG Products Tested

Type	Supplier	Material
203	Allied	silicate
204	Allied	siloxane
305	Allied	siloxane
208	Allied	siloxane
IC1-200	Futurrex	siloxane
DC4	Futurrex	siloxane
ILD	Stauffer	high-carbon siloxane
123	Filmtronics	siloxane
801	Filmtronics	siloxane
802	Filmtronics	siloxane

Several SOG products have been tested as listed in table 3.1. SOG-203 from Allied

Company is one of the original spin-on glasses. The main ingredient is silicate ($Si(OH)_4$) dissolved in an organic solvent. This material can be converted to SiO_2 at a relatively low temperature (about 300-400°C). But the film is porous and, therefore, has very high etch rates in buffered HF solution. SOG-203 is usually used when high temperature annealing is allowed (e.g. over polysilicon topography). The maximum film thickness for most silicate SOG materials is about 3000-4000Å before cracking. Therefore, silicate has been mostly replaced by the siloxane-type SOG, which has a much higher crack resistance. SOG-204 and SOG-305 are both polysiloxane SOG in organic solvents with their respective organic groups attached to the silicon atoms. SOG-204 is recommended for the etch-back planarization process by Allied Company. The annealing temperature needed to convert 204 to SiO_2 is higher (about 500 - 600°C) than most other SOGs, while SOG-305 can be annealed to SiO_2 at a lower temperature (about 400°C). When 305 is used as a planarizing film, "gapping" (separation of the SOG from the substrate) sometimes occurs. SOG-208 is a mixture of 204 and 305, thus, containing the organic groups in both SOGs. The properties of 208 are also averaged over the properties of 204 and 305. After 400°C annealing, the film is not completely converted to SiO_2 as 305. But most of the organic groups (carbon) are removed from the film and no adhesion problems have been reported when using 208 over PECVD oxynitride. SOG-208 will be one of the materials under more detailed study in later sections.

The SOG IC1-200 from Futurrex Company is also a polysiloxane type SOG. Some additives in the film, such as the levelling agent and the adhesion promoter, make the coating properties better than other SOGs. The film thickness is more uniform and no striation effects are seen. This SOG will also be investigated in detail later. DC4 is a thick SOG from Futurrex Company. A spin speed of 3000 rpm can give a 6000 Å film after annealing. It has similar dielectric properties (e.g dielectric constants) to SOG-208 from Allied Company and the film tends to crack over topography. Consequently, DC4 has not been studied in detail.

Stauffer Chemical Company provides a thick SOG, ILD (Inter-Layer Dielectric), which can give close to a 1μm film after coating. This SOG contains a lot of carbon after low

temperature annealing. The film cracks after annealing at 450°C and 600°C and shrinks to one-half of its original thickness after 900°C. SOGs from Filmtronics Company are also polysiloxane type SOG. Their dielectric properties have been studied and differ little from those of the SOG-208 type SOG.

C. CVD dielectric films

After SOG coating, another layer of CVD film is usually needed to complete the 0.6-1.0μm interlayer dielectric film. Both low-temperature low-pressure CVD oxide (LTO) and plasma-enhanced CVD (PECVD) oxide have been tested. The LTO is deposited using a Tylan LPCVD furnance at 450°C at 400 mTorr. The source gases are SiH_4 and N_2O, with the doping gas, PH_3, turned off. The deposition rate of the undoped oxide film is about 1.0μm/hour. The etch rates of the LTO film in buffered HF solution (10:1 = NH_4F:HF) and in the CHF_3 plasma are summarized in table 3.2. The wet etch rate is about 50% higher than that of thermal oxide. This indicates the porosity of the film and a densification step at a higher temperature can reduce the wet etch rate.

Table 3.2 The Etch Rates of Oxide Films

	Etch rate in 10:1 BHF	Etch rate in Technics Plasma Etching Sys.*
LTO	.12μm/min.	.04μm/min.
PECVD	.04μm/min.	.04μm/min
Thermal oxide	.04μm/min.	.04μm/min

* Etching conditions:
CHF_3 = 9 sccm
O_2 = 1 sccm
Power = 100 Watts

The PECVD oxide film is deposited using a Technics PECVD system. This machine generates a 30KHz plasma over a disk area of 300mm in diameter. The deposition temperature

is 250°C on the substrate, the pressure is 400 mTorr and the power is 30 Watts. The source gases are also SiH_4 and N_2O (SiH_4 : N_2O = 2 : 3). The deposition rate is about 1.2μm/hour. Due to the limited area, no more than four wafers can fit into the chamber. The etch rates (listed in table 3.2) are much closer to those of thermal oxide, indicating the film is less porous.

3.2.2 Experiment Descriptions

All of the SOG samples are prepared using a Headway manual photoresist spinner. For each coating, about 3 c.c.'s of spin-on glass is dispensed onto a 100 mm Si wafer. This is followed by a 3000 rpm spin cycle for 20 seconds. Two baking cycles in a VWR convection ovens (120°C for 30 minutes and 200°C for additional 30 minutes) are used to drive the casting solvent from the film to complete the SOG film preparation. These SOG films are then annealed in a Tylan furnance under various conditions to study the effects of annealing on the film properties. The annealing temperature ranges from 400°C to 950°C, with two ambients: oxygen or nitrogen. For the material studies, the samples are analyzed following the anneal. For the dielectric studies, a sputtered aluminum film is patterned to form the electrodes on top of the annealed SOG films.

The film thickness is measured with a Nanospec AFT and the refractive index measured with a Gartner ellipsometer. A Fourier Transform Infrared (FTIR) spectrophotometer is used to measure the IR absorption spectra of the films. Room-temperature stress is measured using an optically levered stress gauge (OLSG).[15-16] Another specially designed hot-stage stress gauge (HSSG) is used to determine the in-situ stress variation during annealing. The capacitances with the spin-on glass film as the dielectric are measured with an HP 4275A multi-frequency LCR meter. The dielectric constant is calculated from the capacitance, the electrode area, and the film thickness.

3.3 Coating Properties

During the initial stage of spinning, most spun-on films display decreasing thickness with time as more material is removed from the wafer. The thickness will saturate at a constant value after a finite amount of spinning time (e.g. about 8-10 seconds for a normal photoresist.) It is desirable to operate the process in the saturation regime to have reproducible results. The film thicknesses of SOG-208 and IC1-200 are plotted against the spinning time in Fig.6. The thickness is essentially constant from a spinning time of 5 seconds to 30 seconds. Compared to other polymer films, the SOGs reach the final thickness in a much shorter time. The low viscosity and high vapor pressure of the solvent can explain this short settling time according to the coating model proposed by Flack et al [10]. Because of the low viscosity, most of the excess liquid is spun off the wafer in a shorter time; the high vapor pressure causes the solvent to leave the film at a higher speed. According to the model, both effects tend to shorten the time when convection loss dominates the change of thickness and enter the time regime when solvent evaporation dominates the thickness change. The solvent evaporation depends on the material properties and is weakly dependent on the spinning time. Consequently, the film thickness stays constant after a short spinning time. Based on Fig.6, a spinning time of 20 seconds is chosen for later experiments.

For any given SOG, the most commonly used method to change its thickness is by varying the spinning speed. Fig.7 shows the film thickness after 200°C bake versus spinning speeds for SOG-208 (Fig.7(a)) and IC1-200 (Fig.7(b)). Over the range between 2000 rpm and 6000 rpm, the thickness of SOG-208 can be predicted by

$$t = \frac{3018}{w^{0.39}} \quad \text{Å}, \tag{7}$$

and that of IC1-200 by

$$t = \frac{3000}{w^{0.44}} \quad \text{Å}, \tag{8}$$

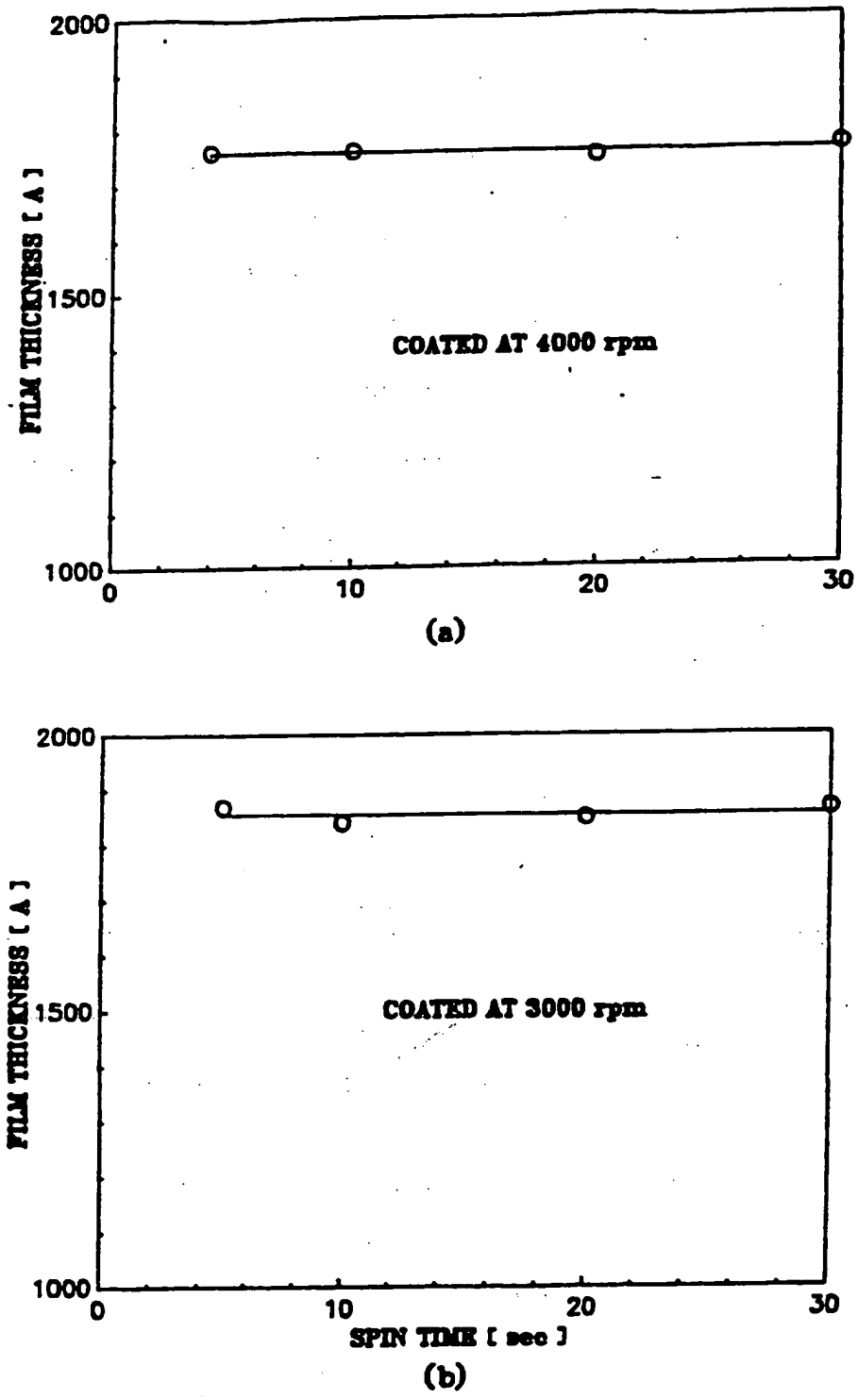
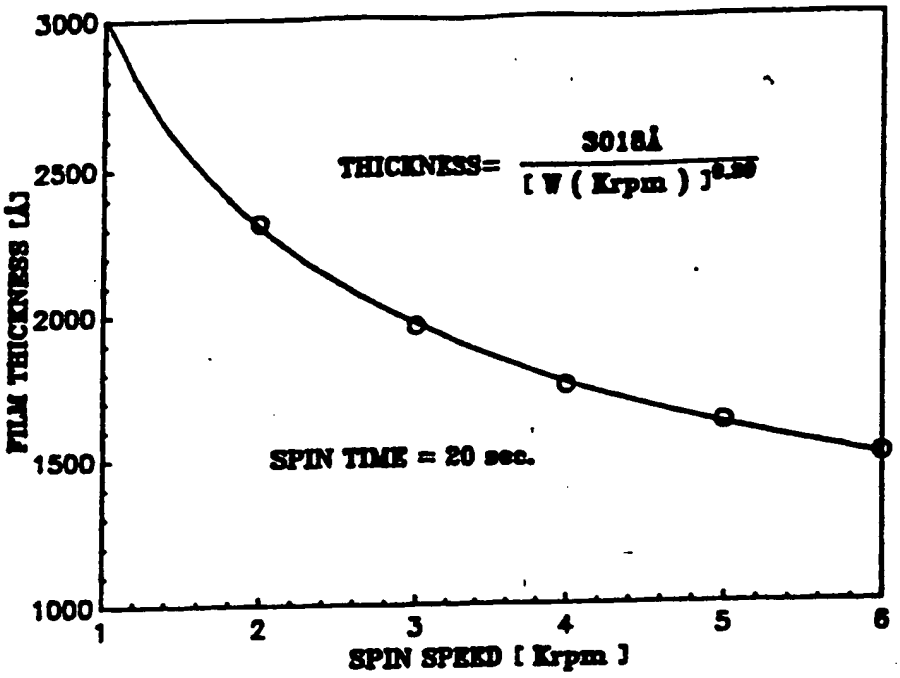
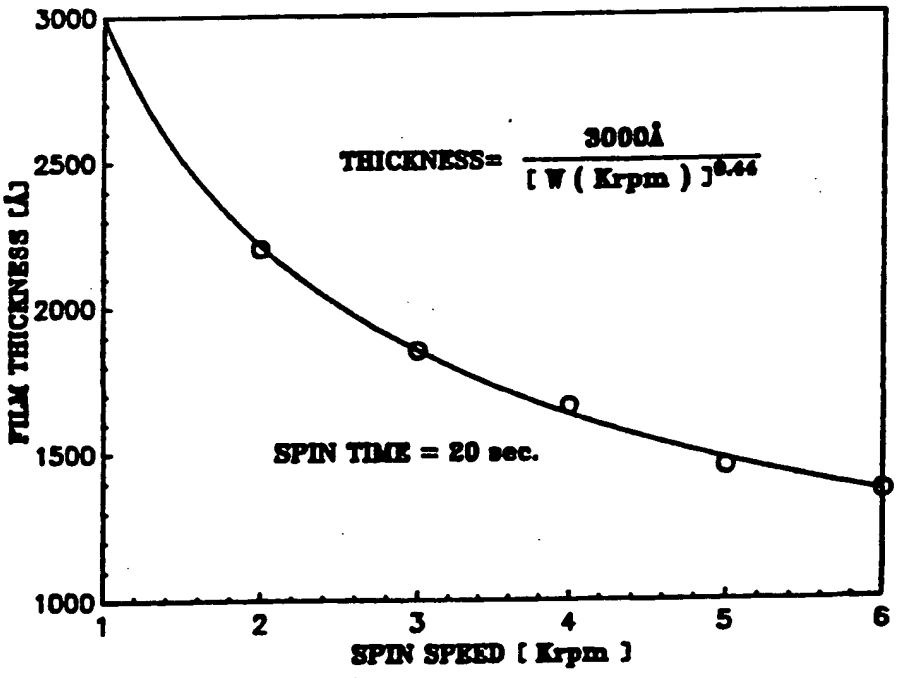


Fig.3.6 The film thickness versus the spinning time for (a) SOG-208 and (b) IC1-200.



(a)



(b)

Fig.3.7 The film thickness versus the spinning speed for (a) SOG-208 and (b) IC1-200.

where w is the spinning speed in 10^3rpm. As can be seen from Fig.7, for a given SOG material, the range of film thickness is limited. If a much thicker (thinner) film is desired, either another SOG with a higher (lower) viscosity and/or higher (lower) solid contents should be used. Multiple-coating is another way to increase the film thickness.

All the data in Fig.7 are taken after 200°C bake. The following high temperature annealing will further decreases the film thickness. Table 3.3 lists the shrinkage factor (defined as the film thickness after a 30-minute 400°C annealing divided by the thickness after 200°C bake) for both SOG's in N_2 and O_2 ambients.

Table 3.3 The Shrinkage Factors of SOG's After Annealing

SOG	Annealing ambient	
	N_2	O_2
SOG-208	.92	.71
IC1-200	.98	.93

SOG-208 shows more shrinkage than IC1-200 in both ambients, and O_2 ambient introduces more shrinkage than N_2 does for both SOG's.

3.4 Material Properties of Some Spin-On Glasses

3.4.1 IR spectra.

The FTIR absorption spectra of bare silicon wafers were measured using a Nicolet 60SX FTIR. The digitized spectra are stored on a hard disk. The 0.22μm SOG films are spin-coated onto a wafer, subjected to cure at 200°C, and the FTIR spectra measured. The films are annealed at 450°, 600° and 900°C in different ambients and the FTIR spectra retaken. Special features due to the substrate are eliminated by subtracting the appropriate bare wafer spectrum from the SOG-coated spectrum. The IR spectra of SOG-208 after 200°C baking is shown in Fig.3.8 with each major peak labeled. The spectra after annealing at 450°C, 600°C and 920°C

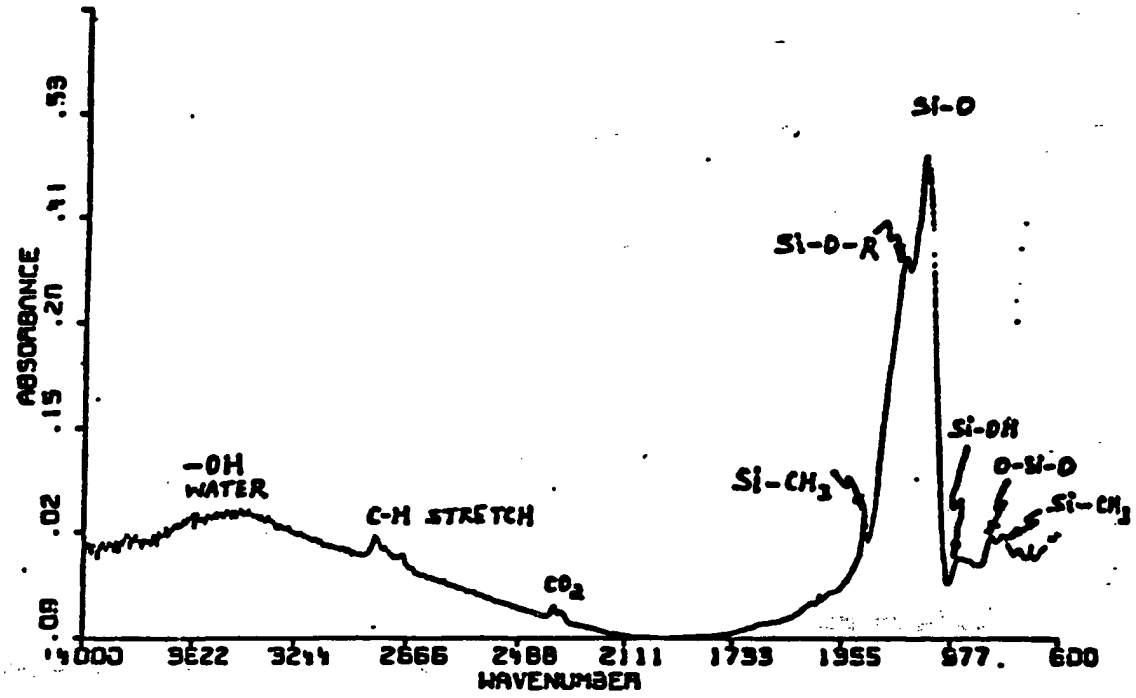


Fig.3.8 Tge IR spectrum of SOG-208 after 200°C bake.

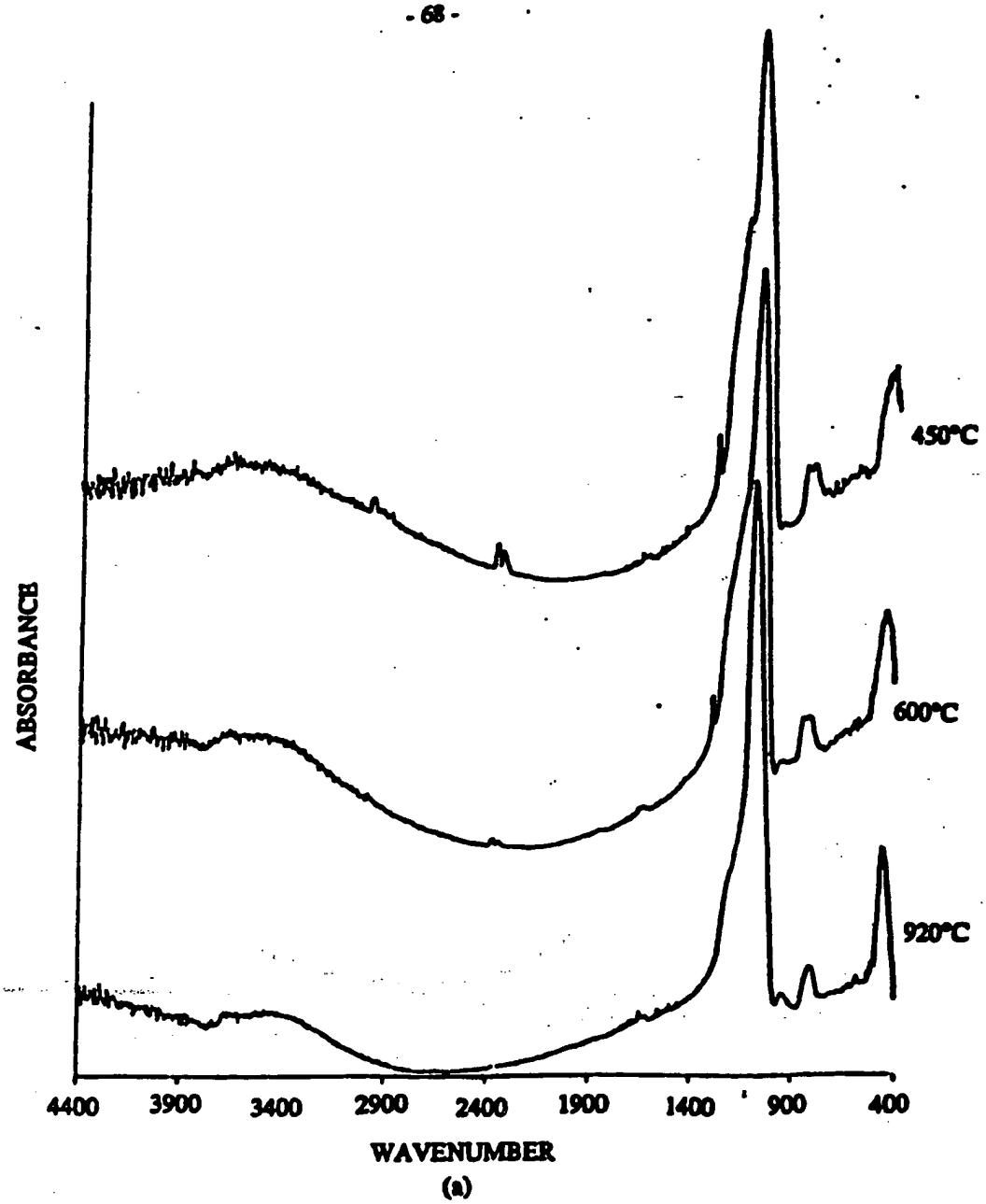
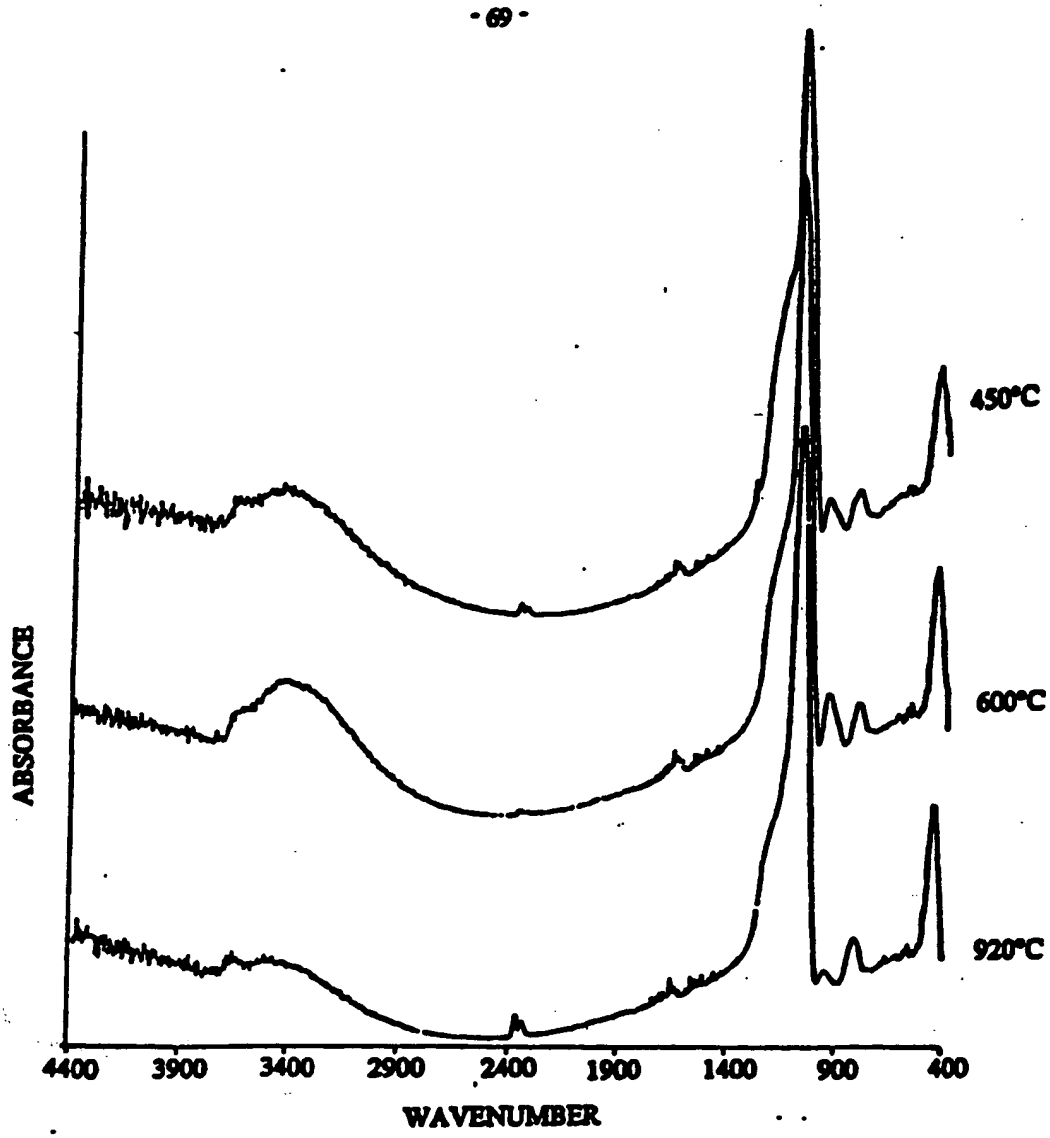


Fig.3.9 The IR spectra of SOG-208 after annealing in (a) N_2 and (b) O_2.


450°C
600°C
920°C
ABSORBANCE
4400
3900
3400
2900
2400
1900
1400
900
400
WAVENUMBER

(b)

in N_2 ambient are shown in Fig.3.9(a) for the range between 400 and 4000 cm^{-1}, while Fig.3.9(b) gives the data for samples annealed in O_2 ambient. All the measurements are made at room temperature in a dry nitrogen ambient. The most intense absorption peak of Si-O bonds, due to the asymmetric stretching mode, is located between 1060 and 1080 cm^{-1}. The location of this peak changes with annealing temperature and ambient as shown in Fig.3.10. Both curves shift to lower wave numbers at 450°C and both reverse that shift after annealing at higher temperatures. The initial shift (450°C) is smaller for the sample subjected to the oxygen anneal. The peak for the oxygen-annealed sample shifts to its final position by 600°C, as opposed to the nitrogen-annealed sample, which still has significant shifts between 600°C and 920°C. The results shown in Fig.3.10 are consistent with the more general observation that the oxygen ambient causes compositional changes to occur at lower temperatures than does the nitrogen ambient to be presented below.

There are two absorption peaks associated with OH bonds in the film: the peak at 940 cm^{-1} and the extended region between 3200 and 3800 cm^{-1}. The broader peak between 3200 cm^{-1} and 3800 cm^{-1} is the sum of the absorption peaks associated with the OH bonds, with the absorbed water and remaining solvent, while the 940 cm^{-1} peak arises from the stretch of silicon-bound hydroxyl (silanol). The areas under these two peaks which give the relative concentration of these OH content are integrated by the FTIR system and are shown in Fig.3.11 as a function of the annealing temperature for SOG-208. The OH profile for the O_2 annealed films in Fig.3.11(a) follows closely to the Si-OH profile under the same annealing conditions shown in Fig.3.11(b), indicating the amount of absorbed water/solvent is small. However, using the 920°C data as a reference, the film annealed in N_2 shows a larger absorption peak at 450°C and 600°C in the 3200 - 3800 cm^{-1} ranges compared to the Si-OH peak at 940 cm^{-1}. This shows that the film contains some water/solvent molecules even after 450°C and 600°C annealing. It is worth noting that the OH concentration is consistently lower when annealed in the N_2 ambient than that in the O_2 ambient and the highest absorption occurs after 600°C annealing in O_2. Annealing at 920°C in either ambient reduces the OH content to a low

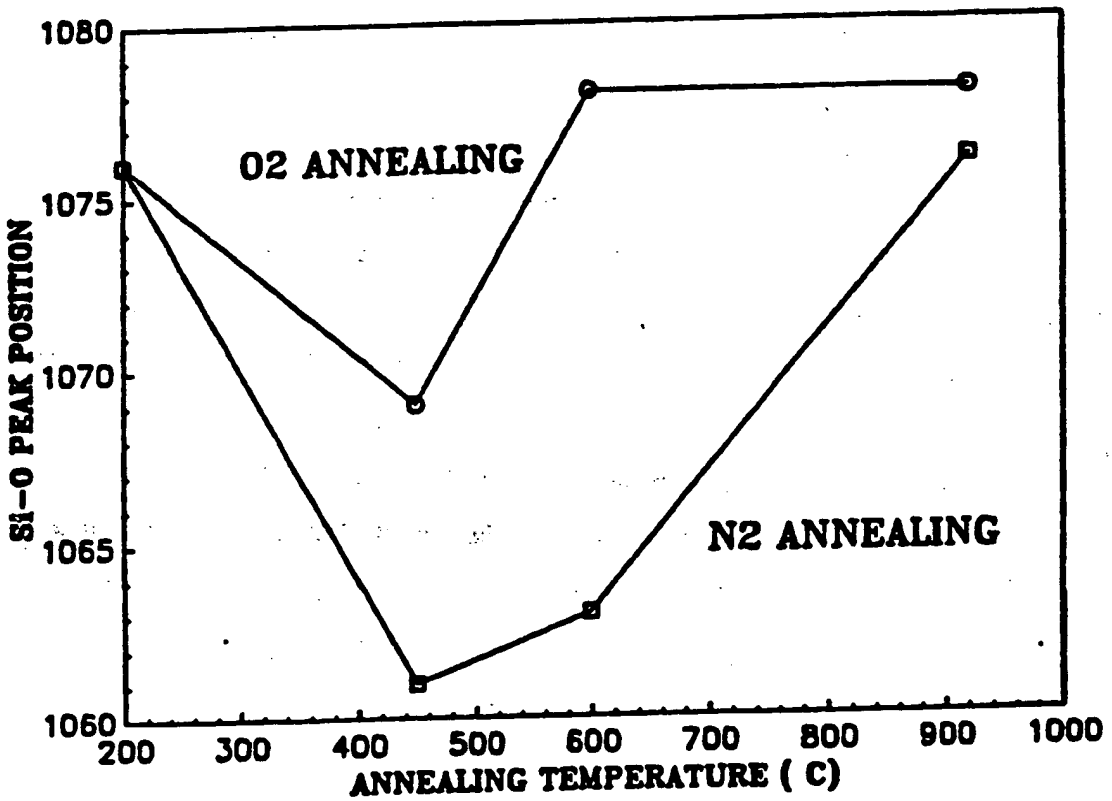


Fig.3.10 Si-O peak positions versus annealing temperatures for SOG-208.

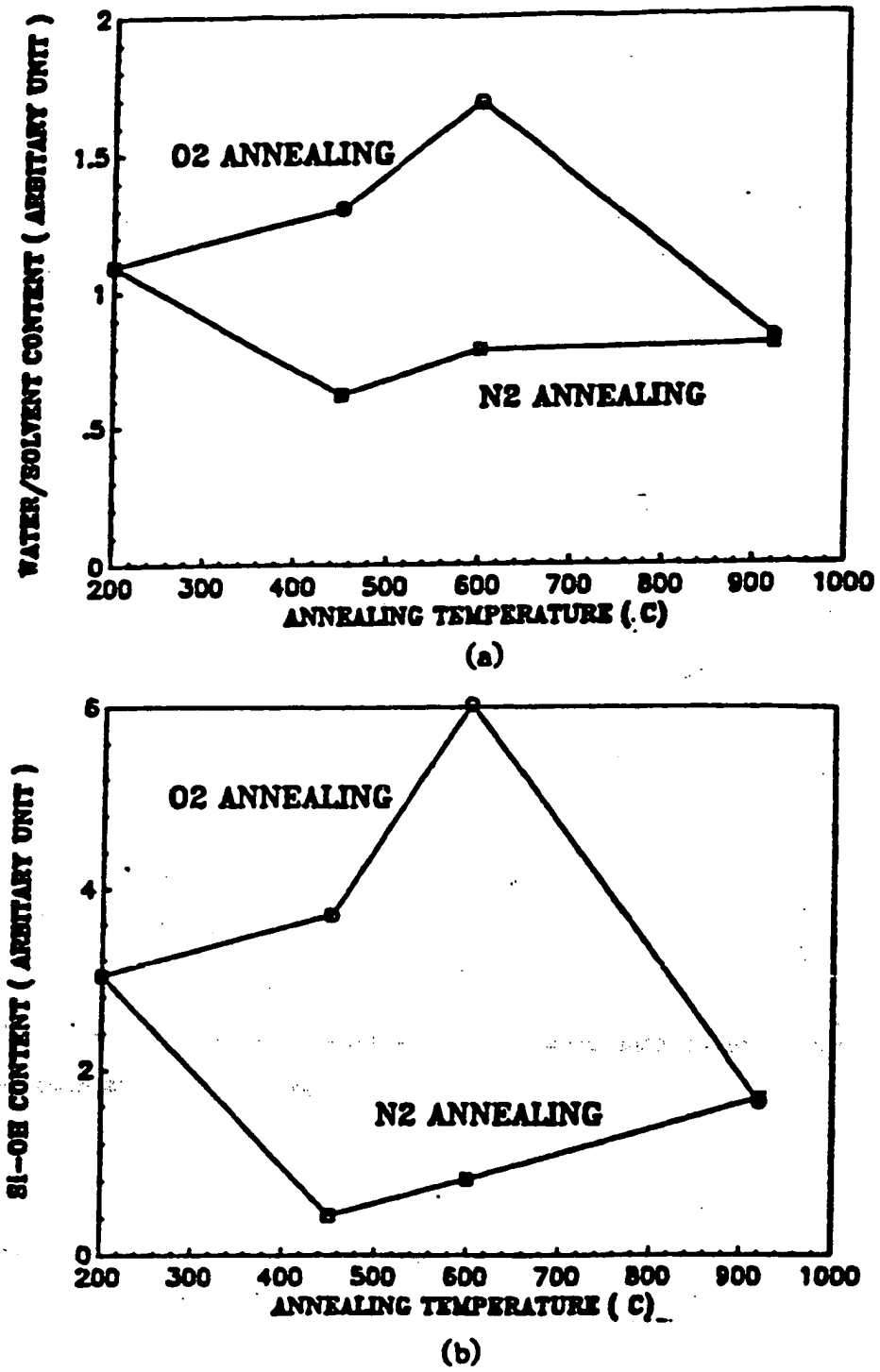


Fig.3.11 Integrated IR peak areas for SOG-208 versus annealing temperatures for (a) the extended OH peak (3200-3800 cm^{-1}) and (b) Si-OH peak (940 cm^{-1}).

level.

One of the main residues in the cured film is the silicon-bound methyl group. The stretching mode of $Si-CH_3$ gives a peak at 1270 cm^{-1} in the IR spectra. The areas under the $Si-CH_3$ peak of SOG-208 films are plotted against the annealing temperature in Fig.3.12. In N_2, the organic group concentration decreases less than 5% after the 450°C annealing. Even after 600°C in N_2 for 30 minutes, more than half the methyl groups remain in the SOG-208 film. All the organics are gone after annealing at 920°C. As previously mentioned, O_2 is a more effective ambient in oxidizing organics. Two thirds of the methyl groups are gone after 30 minutes at 450°C in O_2 and at 600°C or above, almost all of them are gone. The difference between the two annealing ambients in the temperatures required to remove all the organics confirms the observations made from the positional changes of the main Si-O peaks in Fig.3.10.

The complex behavior of the Si-O peak position depicted in Fig.3.10 must be considered in light of all the complicated compositional changes that occur during curing. This is because the presence of water/solvent, organics, and silicon-bound hydroxyl should each have an impact upon the strength of the Si-O polymer bond. The shift of the Si-O peak to lower wavenumbers is attributed to loss of water/solvent due to heating in the 200°C to 450°C range. However, the oxygen ambient is more effective than nitrogen at low temperatures in removing organics and in adding Si-OH. The loss of organics and the addition of Si-OH is assumed to have the effect of shifting the Si-O peak to higher wavenumbers. Thus, while a 450°C anneal in either oxygen or nitrogen causes a shift to lower wavenumbers due to water/solvent loss, the shift is less for oxygen ambient since more organics have been lost and significant Si-OH has been formed as a result. In oxygen ambient, the formation of Si-OH appears to be an important step that mediates the loss of organics at low temperatures, and the formation of glassy SiO_2. The glass formation under nitrogen does not occur until above 600°C. In this case, Si-OH formation may not be a significant intermediate step.

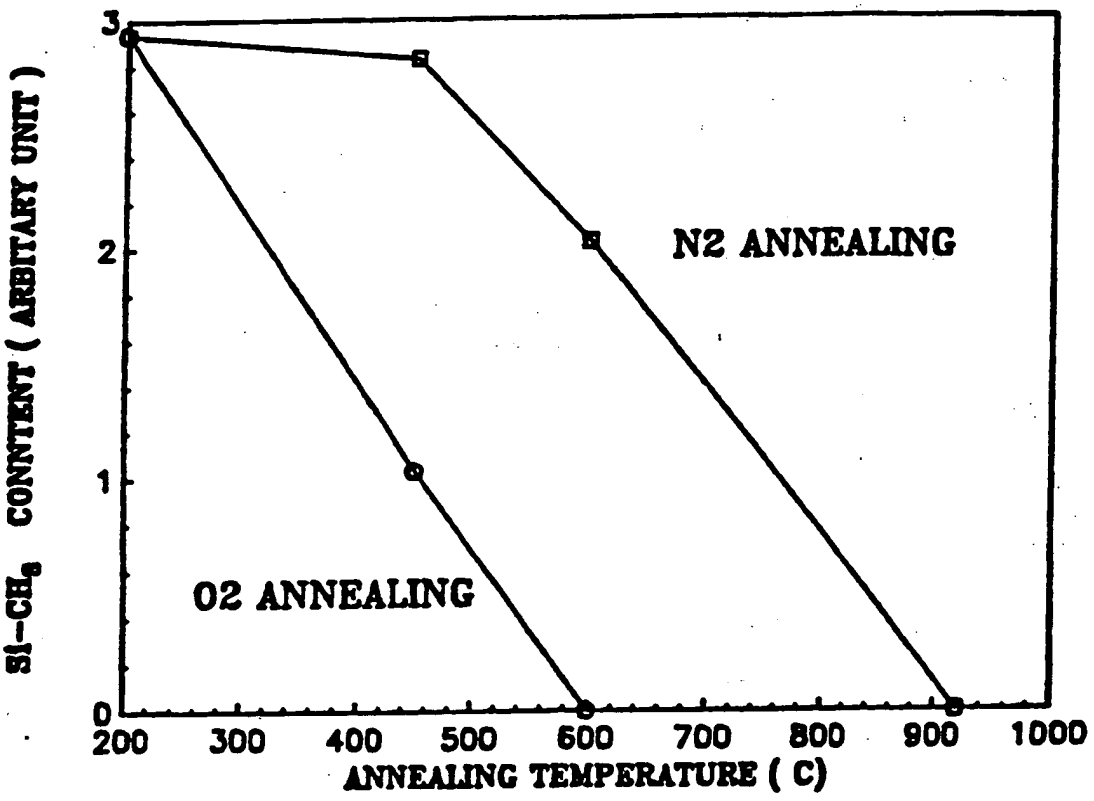


Fig.3.12 Integrated Si-CH_3 peak areas for SOG-208 versus annealing temperatures.

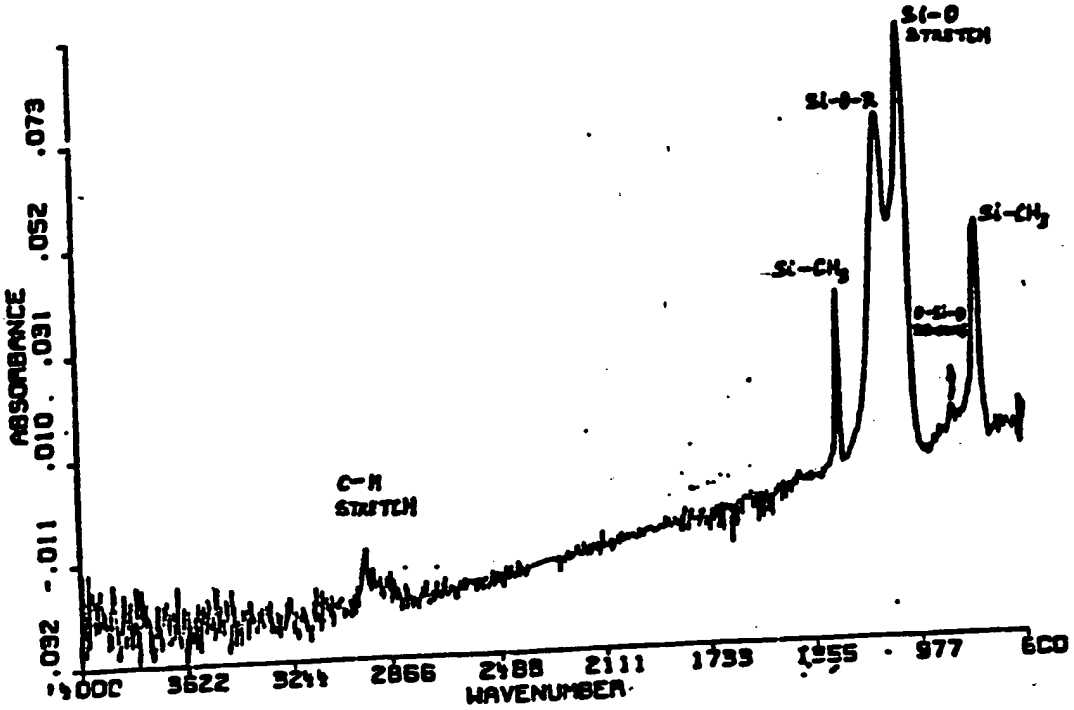
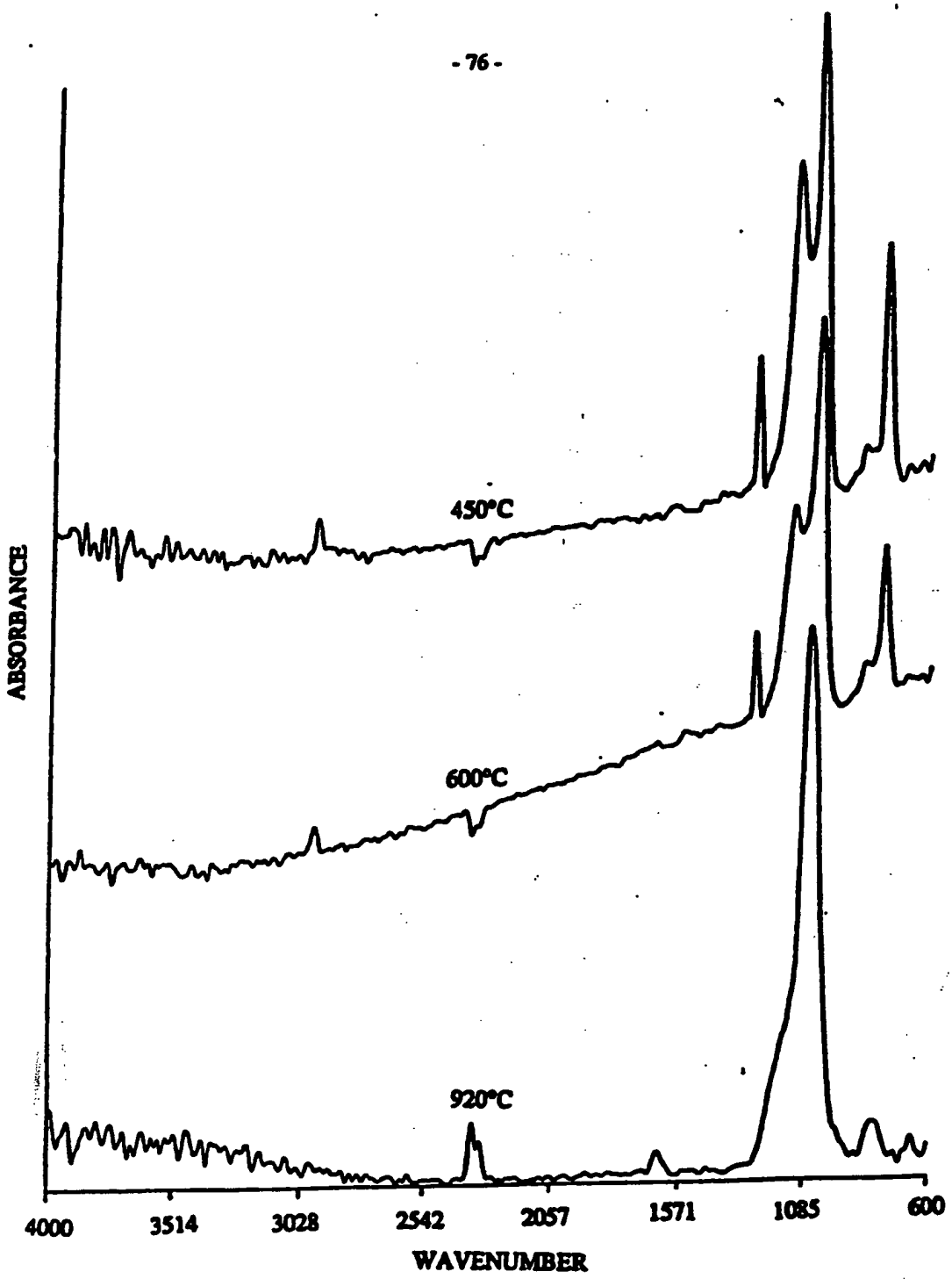
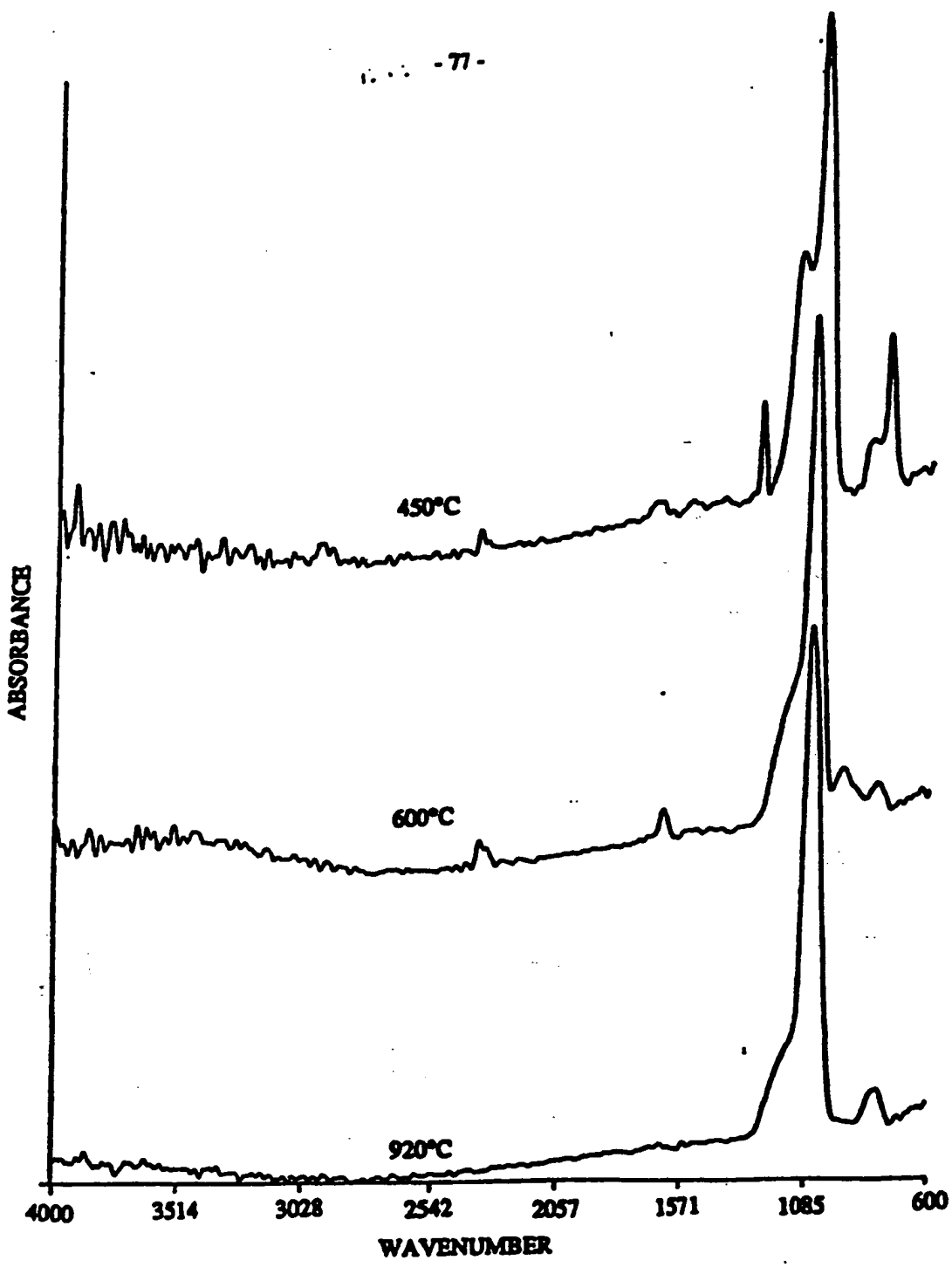


Fig.3.13 The IR spectrum of IC1-200 after 200°C bake.



(a)

Fig.3.14 The IR spectra of IC1-200 after annealing in (a) N_2 and (b) O_2.


450°C
600°C
920°C
ABSORBANCE
4000
3514
3028
2542
2057
1571
1085
600
WAVENUMBER

(b)

The IR spectrum of IC1-200 after 200°C baking is shown in Fig.3.13. The spectra after annealing are shown in Fig.3.14. The locations of the main Si-O peak for different annealing temperatures and ambients are shown in Fig.3.15. The compositional changes invoked to explain the peak shifts of SOG-208 can be used to explain the behavior shown in Fig.3.15 for IC1-200. It illustrates some significant differences between these two SOG materials. In Fig.3.15, the initial peak position after the 200°C cure is much lower, and the drop upon heating to the 450°C is also much smaller, than that observed for SOG-208. This is probably because all solvent for IC1-200, unlike SOG-208, has been removed by the 200°C bake. Other factors, such as lower initial Si-OH content, may also be playing a role. For IC1-200, the oxygen ambient becomes effective at extracting organics and forming Si-OH bonds at temperatures above 450°C. This causes the observed shift to higher wavenumbers. A similar effect of the nitrogen ambient does not begin until temperature is greater than 600°C, and glass formation may not be complete, even at 920°C. Generally, SOG-208 and B differs markedly in their solvent/polymer interaction.

As can be seen from Fig.3.16, the OH content is very low after 450°C annealing in either an O_2 or N_2 ambient. At 600°C, only O_2 annealing increases the OH concentration. Annealing at 920°C in O_2 can remove most of the OH groups from the film. The OH content remains low for all annealing temperatures in a N_2 ambient. The organics (Fig. 3.17) are all gone in an O_2 ambient at an annealing temperature of 600°C or higher. However the N_2 ambient cannot oxidize all of the CH_3 groups until 920°C. This is consistent with the interpretation given for Fig.3.15.

The IR spectra of IC1-200 are more sensitive to the annealing ambients for the temperature range studied than those of SOG-208: O_2 seems more effective in converting the IC1-200 film into SiO_2 than N_2. Since aluminum metallization limits the processing temperature to 500°C or lower, IC1-200 can provide a stable film with very little OH concentration with a 450°C annealing in O_2. This is important since the polar OH groups will respond to a.c. signals and thus increase the dielectric constant. If high temperatures are allowed, such as 920°C,

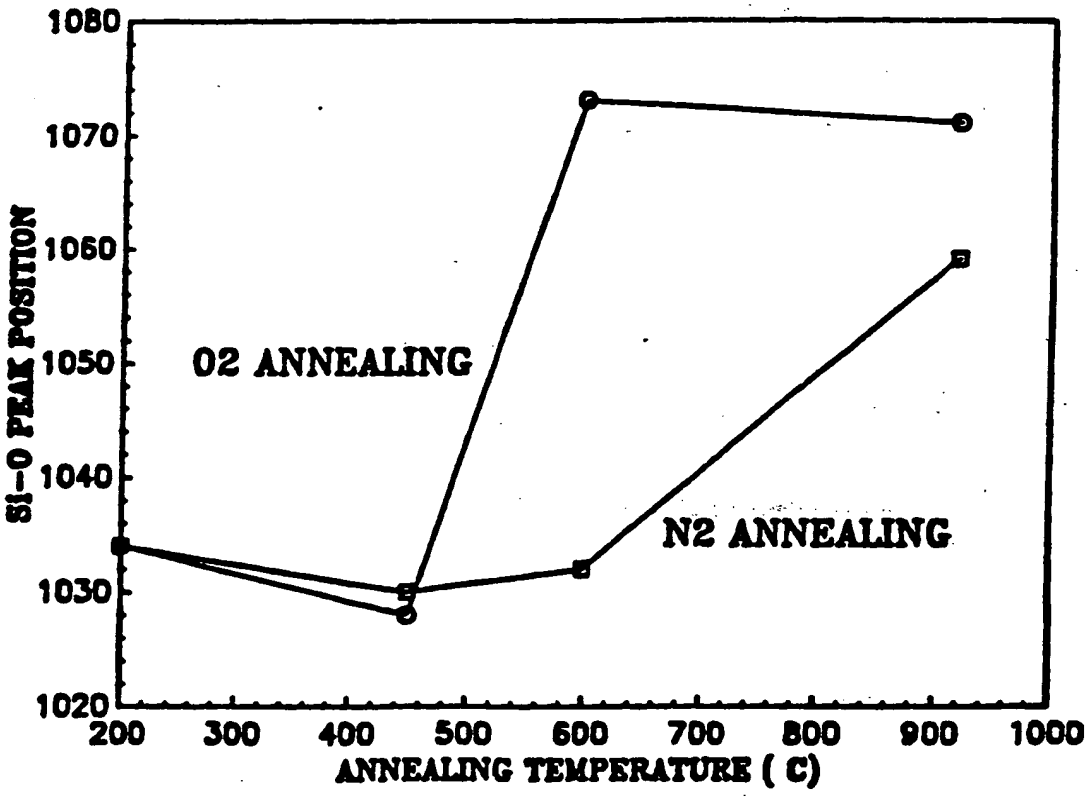
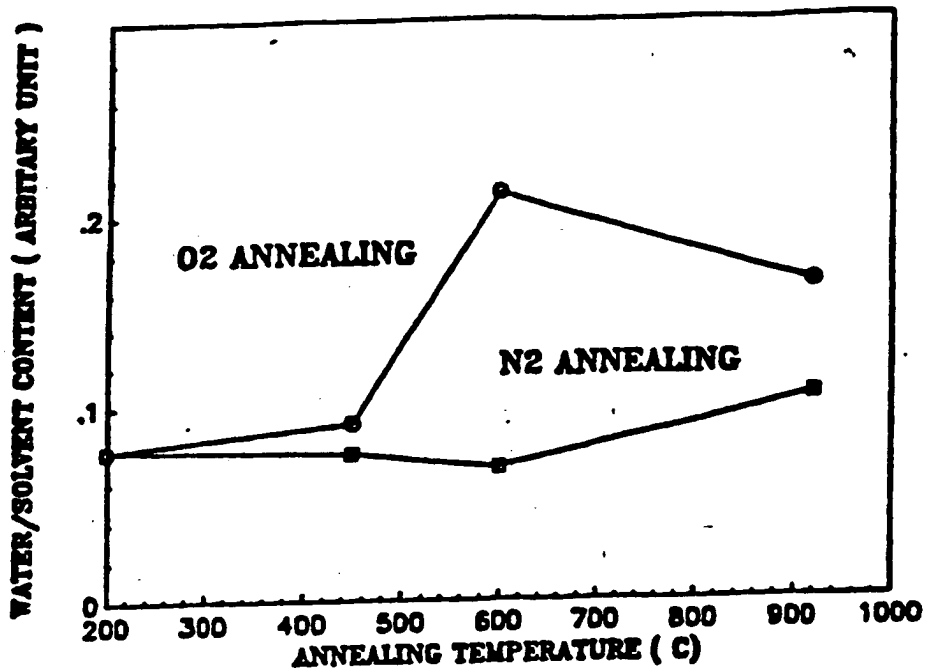
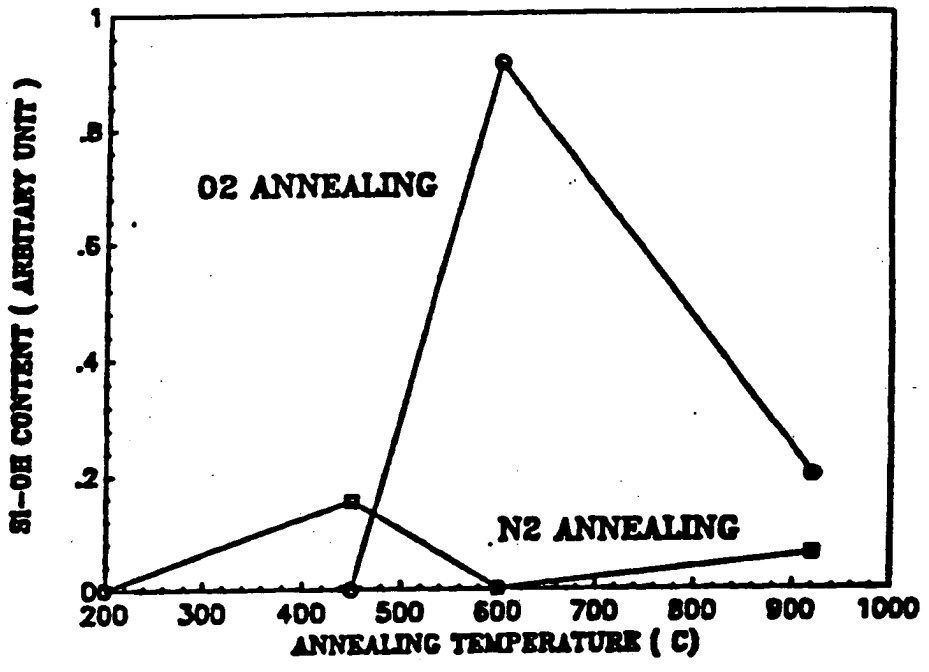


Fig.3.15 Si-O peak positions versus annealing temperatures for IC1-200.



(a)



(b)

Fig.3.16 Integrated IR peak areas for IC1-200 versus annealing temperatures for (a) the extended OH peak (3200-3800 cm^{-1}) and (b) Si-OH peak (940 cm^{-1}).

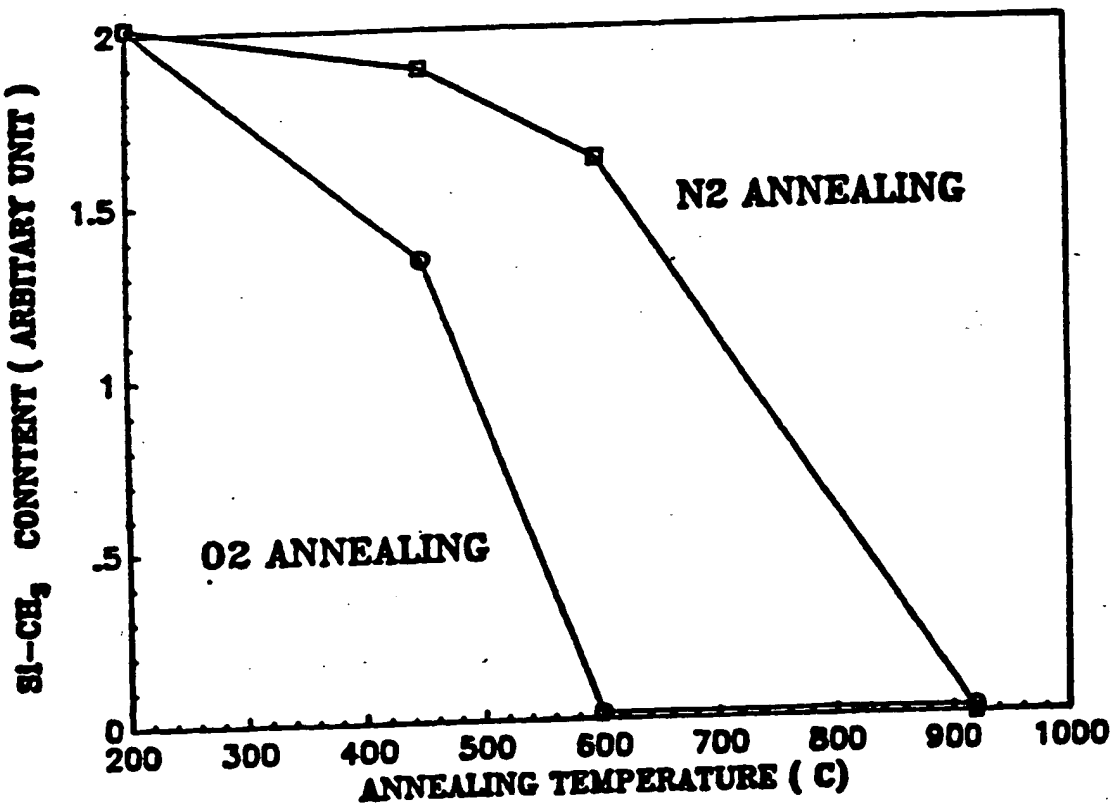


Fig.3.17 Integrated Si-CH_3 peak areas for IC1-200 versus annealing temperatures.

both films possess good material properties.

3.4.2 Stress Measurement.

Two stress measurement systems have been used to study the mechanical behavior of spin-on glass films: a room temperature optically levered stress gauge (OLSG) for observing the films after annealing, and a hot stage stress gauge (HSSG) that permits in-situ measuring of stress during annealing. In both systems, the radius of curvature of a wafer is measured by an optical lever and the bare wafers are measured prior to film deposition to eliminate the contribution of inherent wafer warpage. For the OLSG room temperature system, a laser beam is reflected from the wafer as the wafer is translating across the beam spot and detected by a PIN diode mounted on the translating stage. The radius is calculated from the displacement of the reflected beam. The same process is repeated at several points on the wafer to improve accuracy. The in-situ HSSG system uses an oscillating mirror to scan a laser beam over the wafer surface instead of moving the wafer on a track as in the room temperature stress measurement system. The wafer is held stationary on a hot plate in the HSSG stress measurement system, and is separated from the cool ambient by a ceramic lid, which has a narrow slit that allows the laser to scan across the wafer.[11] This system has a sensitivity for measuring the radius of curvature up to 3 Km.

For a Si wafer with a small amount of wafer warpage, the stress in the film is given by[12] :

$$\sigma_f = \frac{E_s}{6(1-\nu_s)} \frac{t_s^2}{R t_f} \qquad (9)$$

where t_f is the film thickness, R is the radius of curvature, t_s is the Si substrate thickness, E_s is the Young's modulus of Si substrate (with a value of $1.689 \times 10^{11} N/m^2$), ν_s is the Poisson's ratio of the substrate (with a value of 0.064). The stress is tensile (positive in sign) if the warpage is concave on the coated side and is compressive (negative in sign) if convex.

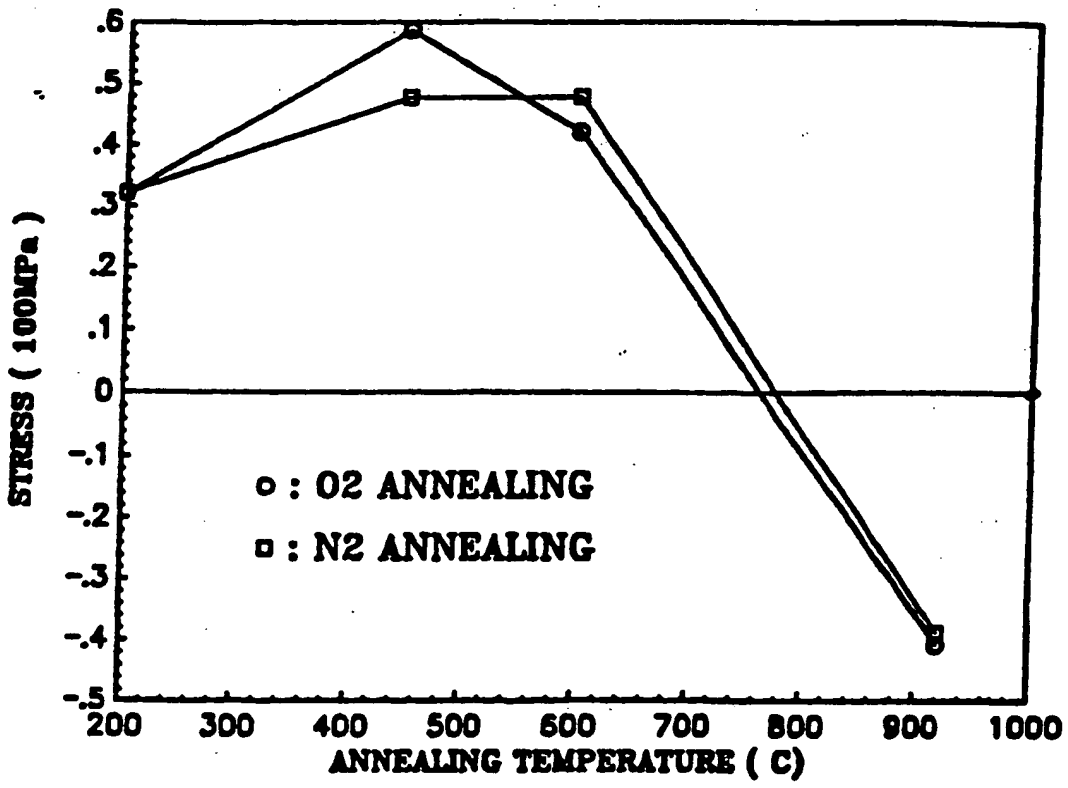


Fig.3.18 Room temperature stress of SOG-208 versus annealing temperatures.

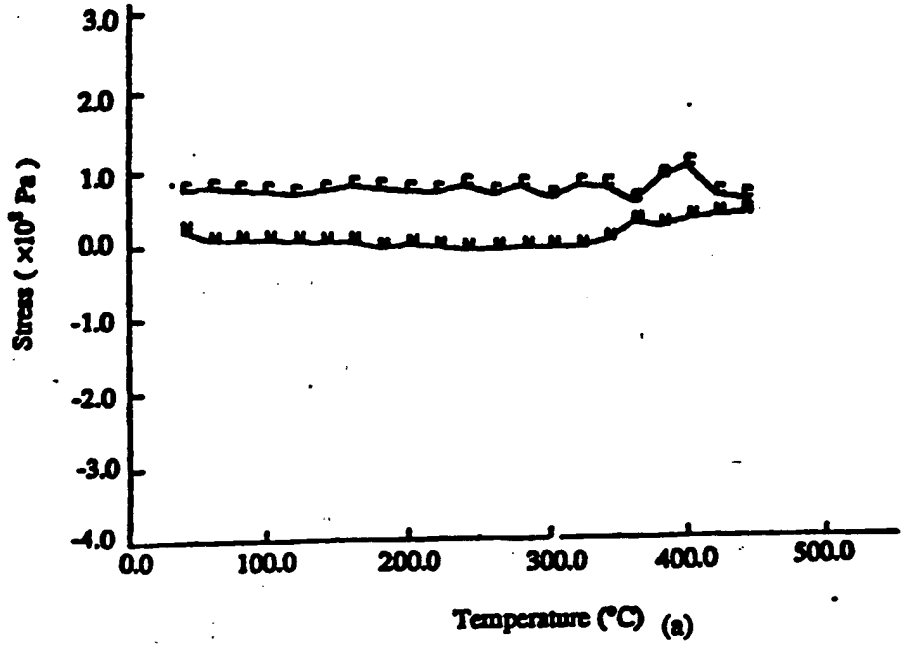
Typical results obtained from room temperature stress measurements of 6000 Å thick SOG-208 films are shown in Fig.3.18. The stress is low for all the samples annealed in different conditions (less than 10^8Pascal.) The tensile stress increases after 450°C annealing as compared to the as prepared film with 200°C bake. This is due to additional film shrinkage at higher annealing temperatures. After 920°C annealing, the film shows a low compressive stress at the room temperature. The results of room temperature stress measurements for IC1-200 give similar results and the stress level is slightly lower than that of SOG-208.

Fig.3.19 shows the in-situ stress measurements of a 4000 Å thick IC1-200 film for two maximum temperatures: 440°C and 600°C. The curves labeled H represent the heating cycle with a heating rate of 10°C/min. The C-labeled curves represent the cooling cycle. The cooling rate is 10°C/min down to the chuck temperature of 100°C, then at a much slower rate as the air cooling is less effective below this temperature. The samples are held for 30 minutes at the highest temperatures, 440°C in (a) and 600°C in (b) between the heating cycle and the cooling cycle. Holding the film at the high temperature increases the tensile stress. The increase is larger for higher temperatures. During the cooling, the stress does not change at all. It remains almost the same stress level as that at 440°C, and is slightly lower than that at 600°C. Again all the stress is relatively low (around 10^8 Pa.) compared to other deposited oxide films of comparable thickness. For IC1-200, the increase in tensile stress at temperature > 200°C is small indicating that additional shrinkage for IC1-200 is small.

3.5 Dielectric Properties of Some Spin -On Glasses

3.5.1 Dielectric constants:

As part of the interlayer dielectric film, the SOG should have acceptable dielectric properties. The dielectric constants (ε_r) of both SOG-208 and IC1-200 have been characterized after various annealing cycles. The dielectric constant is measured using capacitors fabricated on aluminum-coated Si wafers. If a high annealing temperature is desired, a heavily doped Si wafer is used instead of the Al-coated wafer. The thickness of the SOG films is adjusted to



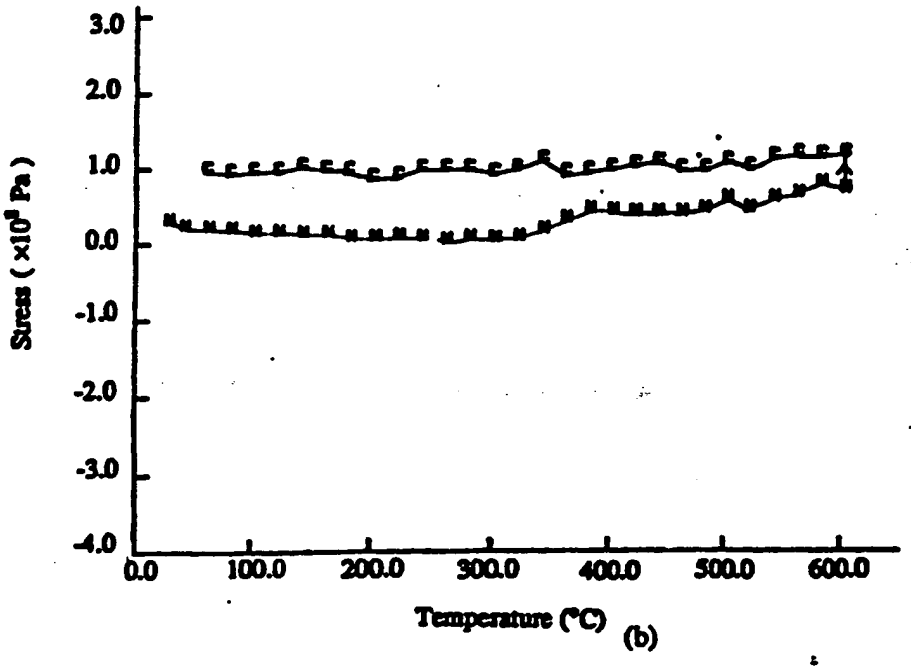


Fig.3.19 In-situ stress measurements of IC1-200 up to (a) 440°C and (b) 600°C.

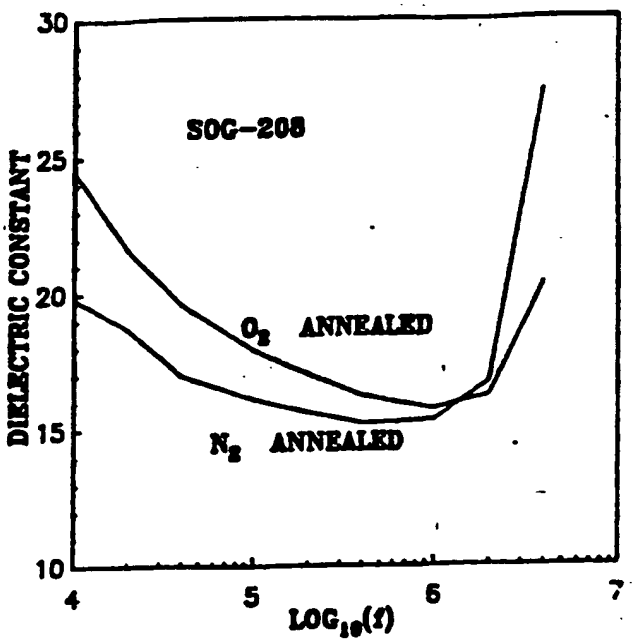
near 2000 Å by choosing the appropriate spinning speed. After the oven bake and the furnance annealing, another layer of aluminum is sputter-deposited and patterned as the top electrode. No special care is taken to keep the wafers from moisture. The capacitance is measured by a HP 4275a multi-frequency LCR meter for the frequency range from 10KHz to 10MHz. For each SOG and annealing condition, 10 capacitors are measured and the averaged data are listed in table 3.4.

Table 3.4 The Dielectric Constants and Dissipation Factors (in parentheses)of SOGs

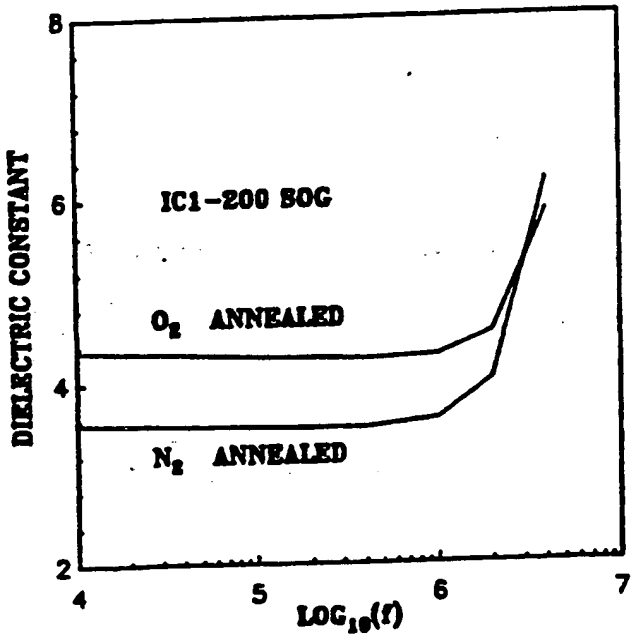
	SOG-208		IC1-200		LTO
Annealing Ambient	N_2	O_2	N_2	O_2	
10KHz	19.8 (.50)	28.8 (.90)	3.55 (.010)	4.35 (.008)	9.2 (.003)
100KHz	16.1 (.14)	16.8 (.31)	3.51 (.009)	4.28 (.012)	9.3 (.039)
1MHz	15.3 (.07)	14.9 (.12)	3.59 (.019)	4.29 (.026)	8.9 (.14)

SOG-208 shows much higher dielectric constants than IC1-200 does for all the annealing conditions. The ε_r values of SOG-208 are several times higher than that of pure silicon dioxide ($\varepsilon_r = 3.9$). The films are leaky at low frequency (10 KHz) as can be seen from the high values of dissipation factors; therefore, it is difficult to measure the exact values of ε_r. But the data show that the dielectric constants are much higher than 3.9 for both annealing ambients. The dielectric constants of IC1-200 are lower and much closer to that of SiO_2. Annealing in an inert ambient (N_2) results a lower dielectric constant than for an oxidizing ambient (O_2). The lower ε_r is attributed to the presence of residual organic groups left in the film.

The effects of frequency on the dielectric constants are shown in Fig.3.20. For SOG-208 (Fig.3.20(a)), the measured dielectric constant decreases as the frequency increases from 10KHz to about 1 MHz. Fig.3.20(b) shows the ε_r values of IC1-200 stay at a constant value for each curve up to above 1MHz.



(a)



(b)

Fig.3.20 The dielectric constants versus the measuring frequencies for (a) SOG-208 and (b) IC1-200.

The dielectric constant is known to have a strong correlation to the moisture content in the film[7]. High H_2O concentration tends to form the highly polarizable Si-OH bonds and thus increase the dielectric constant. SOG-208 is shown to have high moisture in the film after annealing, and the concentration can only be reduced at very high annealing temperature (> 900°C). The moisture content in IC1-200 is shown to be extremely low, especially after N_2 annealing. The measured data in table 3.4 are consistent with the discussion above.

3.5.2 Dissipation Factors.

Fig.3.21 shows the equivalent circuit of a lossy dielectric. The conductance models the leakage mechanism in the film. If a signal V is applied between the two terminals in Fig.3.21, the current would be

$$J = (jwC + G) * V \tag{10}$$

The dissipation factor, defined as the ratio of power dissipated by the conductor to the power stored in the capacitor, is

$$D = \frac{GV^2}{jwCV^2} = \frac{G}{wC} = \frac{\sigma A / t}{w \varepsilon_r A / t} = \frac{\sigma}{w\varepsilon_r} \tag{11}$$

$$= \frac{1}{w\varepsilon_0\rho} \tag{11'}$$

where ρ is the a.c. resistivity at frequency w (= 2f).

For a dielectric used in the multilayer interconnection technology, a high resistivity is desired. The measured dissipation factors for SOG-208, IC1-200 and LTO are also listed in table 3.4 (in parentheses.) The calculated a.c. resistivities are listed in table 3.5. For most cases, the resistivity of SOG-208 is about two orders of magnitude lower than that of IC1-200. Again, this can be related to the fact that the annealed SOG-208 film contains a high moisture content, which is known to generate deep-level traps in the oxide and conduct current. LTO film shows low a.c. resistivity at high frequency (1MHz), possibly due to the moisture

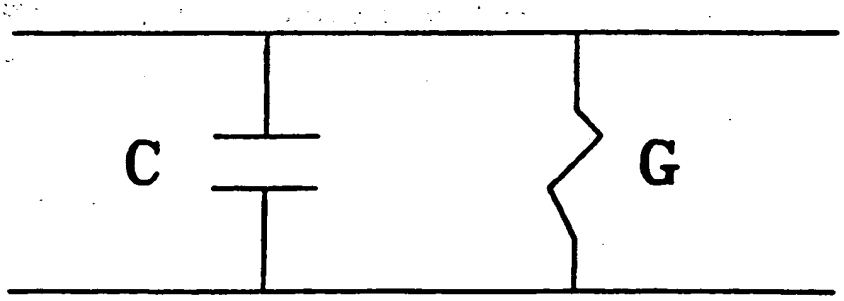


Fig.3.21 The equivalent circuit for a lossy dielectric film.

content in the as-deposited film.

Table 3.5 The A.C. Resistivity ($\rho = \frac{1}{wDc_r}$) of Annealed SOGs (in MΩ-cm)

	SOG-208		IC1-200		LTO
Annealing Ambient	N_2	O_2	N_2	O_2	
10KHz	18	7	5000	5200	6500
100KHz	8	3.5	570	350	50
1MHz	1.7	1.0	26	16	1.4

3.5.3 Breakdown Field.

The breakdown filed distribution measures the defects in a dielectric film. The residual hydroxyl groups and organic groups in the SOG films can generate traps in the oxide bandgap. This research will study the effect of different compositions of SOG films on the defect density after annealing.

The breakdown fields are measured by MOS capacitors fabricated on silicon substrates with the SOG film as the dielectric film. The capacitor areas are all around 1 mm^2. The I-V characteristics of each sample are taken by an HP 4145 curve tracer. Due to the defects in the film, the I-V curves generally show soft breakdown, i.e. current increases smoothly with increasing voltages. Therefore, a critical current of 1 mA/cm^2 is used to define the breakdown field. For each film, 30 capacitors are measured and the results are shown in Fig.3.22.

SOG-208 shows the lowest breakdown field distribution (between 0.5 - 1.0 MV/cm), IC1-200 shows better results (between 2.5 - 3.5 MV/cm) and LTO gives the highest values (above 5 MV/cm). For all the samples, very low currents (less than 10 $\mu A/cm^2$) are measured when the applied voltages are 5 V below the breakdown voltages (~ 20 V for SOG-208, ~ 60 V for IC1-200 and ~ 75 V for LTO.) This indicates that the defect densities are low for all three films at their respective thickness. Both SOG films have very tight distributions of breakdown fields (within +/- 0.5 MV/cm) compared to that of LTO (3 MV/cm difference

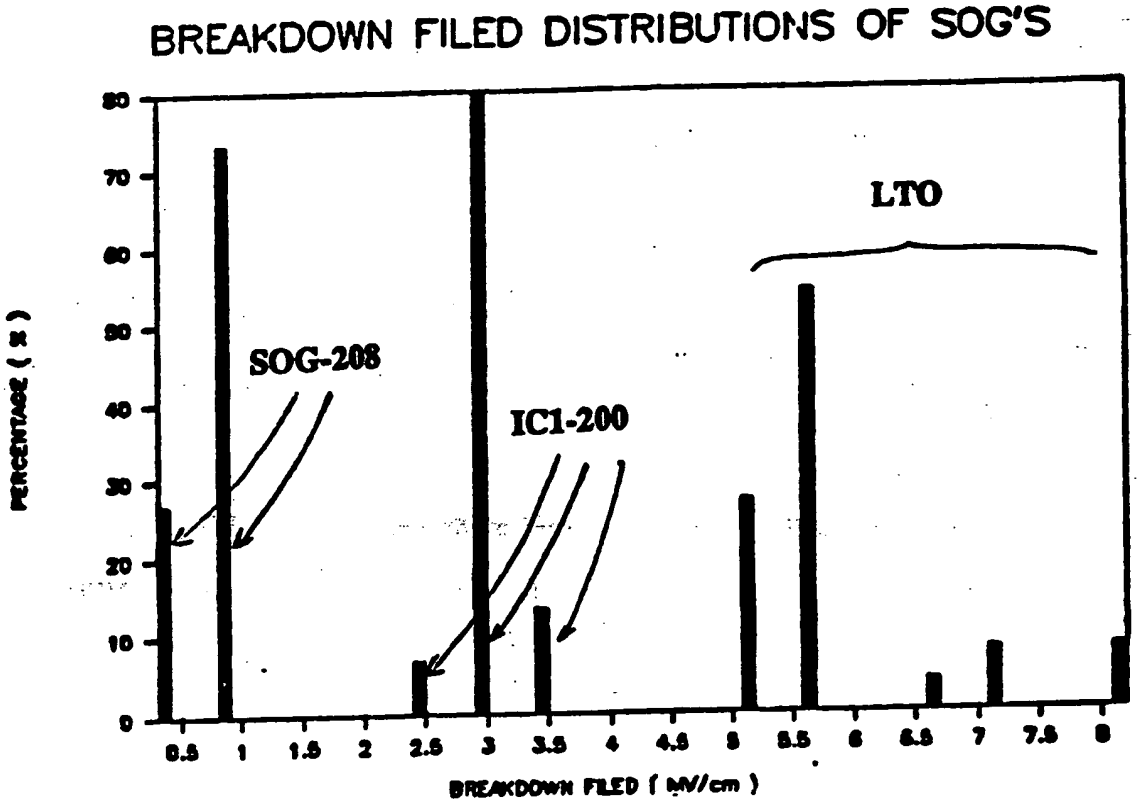
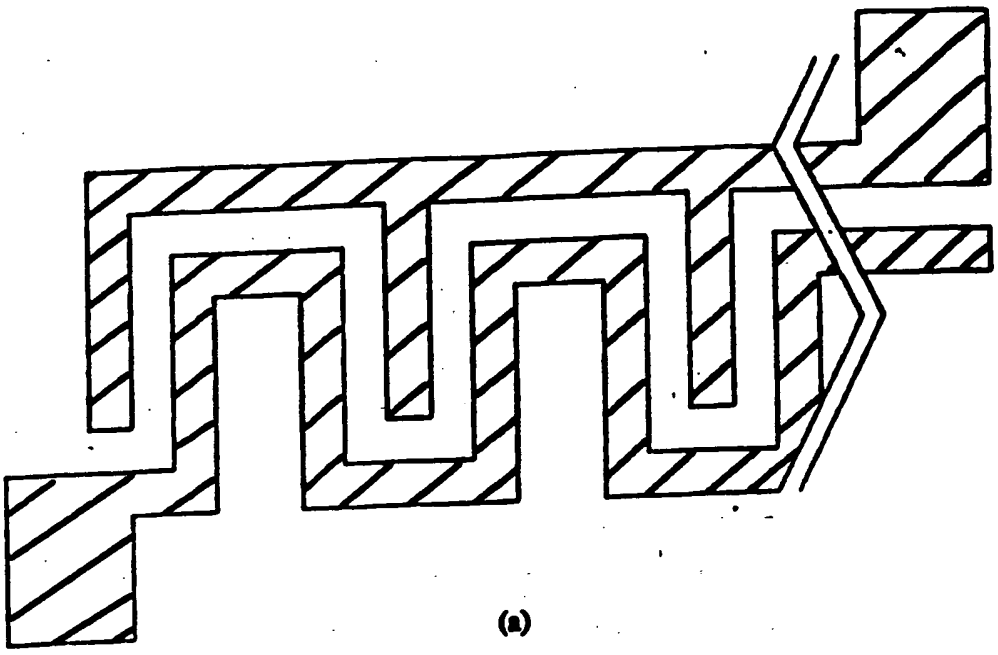


Fig.3.22 The distribution of breakdown fields for SOG-208, IC1-200 and LTO.

between the highest and the lowest values.) The tight distributions suggest that those defects, resulting in low breakdown fields, are homogeneously distributed in these films. The defect density of LTO is so low that the probability of hitting a capacitor with much fewer defects is high enough to show up in the measurement of 30 capacitors. All the breakdown fields measured here are significantly lower than that of pure silicon dioxide (13 - 15 MV/cm). In most multilevel interconnection applications, another dielectric film is added to increase the total thickness and the electrical field encountered is usually less than 10 V/μ (= 0.1MV/cm); therefore, the low breakdown fields of SOG films do not pose serious problems for most applications.

3.5.4 Surface Resistance.

When SOG films are used in multilevel interconnection applications, non-etchback planarization processes are simpler than etch-back processes as mentioned before. An important requirement for non-etchback processes is that the SOG films covering the metal patterns cannot conduct appreciable currents to cause crosstalk in the circuit. The amount of the lateral leakage is measured by the surface resistivity, which is the voltage to current ratio between two parallel conductors. To prepare the experimental samples, sputtered aluminum films of 1 μm thickness are patterned over a 3000 Å oxide film. Then a 2000 Å SOG film is coated, and annealed at 450°C for 30 minutes in N_2. Another 3000 Å LTO film is deposited as the passivation layer. The testing vehicle is a comb-shaped pattern with another serpentine pattern running parallel to the teeth of the comb-pattern (Fig.3.23(a)). The spacing between the two patterns is 2 μm and the total length of these parallel edges is 83 mm. The voltage is recorded at which the current exceeds 1 μA/cm (Fig.3.23(b)). SOG-208 shows very complicated behavior in this experiment. The current density between the two parallel patterns starts to exceed 2.5 μA/cm around 20 V. If the bias is held at this voltage, the current decreases gradually to below 1μA/cm. If the voltage is increased after this "self-curing" process and the current density is kept below 2.5μA/cm, the SOG-208 film can sustain up to 400 V (the

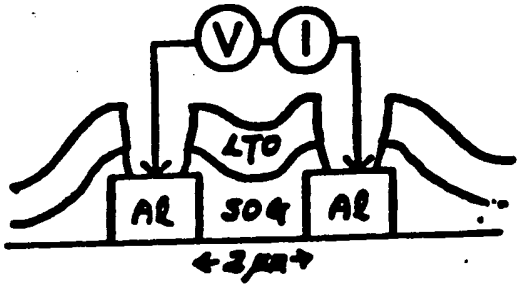


(a)

LATERAL CONDUCTION/ INTERFACE RESISTIVITY

Ic= 1 μA/cm

AG208	30–50V
FUTURREX	>400V



(b)

Fig.3.23 The surface leakage current measurement. (a) The test vehicle is a comb-shaped pattern. (b) The measured data for SOG-208 and IC1-200.

maximum value of the power supply.) The ramping rate of the voltage in this case is usually limited to below 2V/sec.. If the voltage is increased faster, such as 20V/sec., the SOG-208 films breaks down between 30 and 60 V. In this fast-ramping mode, permanent damage is done and the film is leaky after the breakdown (ρ_s < 1MΩ/cm). The IC1-200 film has less complex behavior in the surface resistivity measurement: the breakdown voltages are higher than those of SOG-208 and the I-V curves show a sharp breakdown. More than 40% of the measured data give a surface resistivity higher than $2x10^{12}\Omega/\square$ and all the tested results are higher than $10^{12}\Omega/\square$. For most VLSI circuits operating at a 5V power supply, both SOG-208 and IC1-200 films can provide good isolation between parallel metal lines. But in the applications where voltage spikes much higher than 5V are present, e.g. at the input/output ports, IC1-200 films provide better protection and are less likely to result in permanent damage.

3.5.5 Via resistance

In non-etchback applications of SOG, the Al pad is exposed to the SOG film. Moisture in the glass can affect the deposition of the next layer of aluminum and "poison" the via, resulting in an exceedingly high contact resistance. Both SOG-208 and IC1-200 have been tested in a non-etchback planarization process. No special care is taken to keep the samples from water. In fact a deionized water rinse is performed after every etch step (aluminum, oxide, and resist.) The native oxide on the first layer aluminum in a via is removed by dipping the sample in a standard aluminum etcher for 10 seconds. Then the sample is rinsed, spun dry, and put into the sputter chamber directly. After the deposition and patterning of the second layer metal, a 400°C sintering is performed in forming gas (N_2/H_2). If the dip is omitted prior to the metal deposition, both SOGs show a contact resistance higher than several MΩs per contact. With the dip step in place, SOG-208 still shows a high contact resistance (200 MΩ/contact). A 2μm by 2μm via shows 0.2 Ω per via with the IC1-200 SOG.

3.6 Summary

Both etch-back and the non-etchback planarization processes using spin-on glass have

been examined. It is found that the simple etch-back process is severely challenged when the underlying metal space is less than 1.2μm. For the non-etchback process, the approach of using a dual layer (0.2μm SOG/ 0.6μm CVD oxide) is not effective in improving the step coverage of the following deposition when the underlying metal space is around 1.5μm. Other approaches, such as a thicker SOG film or a sandwich structure, are needed.

The characteristics of two different types of SOG were studied as a function of their annealing temperatures and ambients. It has been established that different annealing conditions are required to optimize the dielectric properties for different SOG materials. The FTIR studies clearly showed the presence and absence of different organic groups after various annealing conditions. It can also be used to determine the presence of bonded OH groups and absorbed OH groups after various annealing conditions. The IR spectra studies show that the OH concentration in SOG-208 films depends strongly on the annealing conditions. An inert ambient (N_2) generally introduces less OH content into the films than an oxidizing ambient (O_2) does. For SOG-208 films, neither annealing at 450°C nor at 600°C can drive off all the OH content. Only after 920°C annealing can the film be dehydrated. However, IC1-200 shows a very low OH content film after 450°C annealing in either O_2, N_2 or steam. The Si-O peak position and shifts observed can be interpreted in terms of the effects that solvent, organics, and silicon-bound OH have upon the Si-O bonding network. IC1-200 after the initial 200°C bake has very little residual water/solvent, in contrast to SOG-208.

The residual stress after annealing as well as in-situ stress during the annealing process have been determined for two different types of SOG materials. The stress levels of both SOG-208 and IC1-200 films are low tensile after half an hour anneal at 450°C and 600°C. The stress is relieved at 920°C and becomes compressive when cooled to room temperature.

The measured dielectric properties of the SOG films are also found to be sensitive to annealing conditions. Furthermore, a good correlation has been established between dielectric properties obtained from electrical measurements to that of OH concentration in the SOG films obtained from FTIR measurements. Dielectric constant and dissipation factor increase with OH

concentrations. IC1-200 films show low dielectric constant, low via resistance and medium breakdown field after relatively low temperature annealings as required by the multilevel aluminum metallization processes. Both films provide good dielectric properties if high temperatures are allowed.

3.7 Reference

[1] F. Dupuis, Y. Shacham-Diamand, W.G. Oldham, " Planarization with Spin-On Glass/LPCVD Composite Film," 1985 Sym. on VLSI Tech., p.52 (1982).

[2] M. Nakamura, R. Kanzawa, "Stress and Density Effects on Infrared Absorption Spectra of Silicate Glass Film," J. Electrochem. Soc., vol. 133, p.1167, (1986).

[3] G.E. Whitwell, " The Performance and Processing of a New Spin-on Polysiloxane Interlevel Dielectric Material," Proc. IEEE VLSI Multilevel Interconn. Conf., p.292, (1986).

[4] S.K. Gupta, S.W. Kirtley, C.B. Vines, " Interlevel Dielectric Planarization with Spin-on Glass Films," Proc. IEEE VLSI Multilevel Interconn. Conf., p.506, (1986).

[5] P. Elkins, K. Reinhardt, R. Tang, " A Planarization Process for Double Metal CMOS Using Spin-On Glass as a Sacrificial Layer," Proc. IEEE VLSI Multilevel Interconn. Conf., p.102, (1986).

[6] J. Multani, J. Chu, S. Mittal, J. Orton, " Spin-on-Glass Dielectric Planarization for Double Metal CMOS Technology," Proc. IEEE VLSI Multilevel Interconn. Conf., p.474, (1986).

[7] P.L. Pai, A. Chetty, R. Roat, N. Cox, C. Ting, " Material Characteristics of Spin-on Glass for Interlayer Dielectric Applications," submitted to J. Electrochem. Soc..

[8] C. Ting, R. Roat, N. Cox, "Spin-on Glass as a Planarizing Dielectric Layer for Multilevel Metallization," The *ECS* Fall Meeting Abstract # 352 (1986).

[9] W. G. Oldham, A. R. Neureuther, C. Sung, J. L. Reynolds and S. N. Nandgaonkar, "A General Simulator for VLSI Lithography and Etching Processes: PartII-Application to Deposition and Etching," IEEE Trans. on Electron Devices, Vol. ED-27, No. 8, pp. 1455-1459, August 1980.

[10] W.W. Flack, et al,"A Mathematical Model for Spin Coating of Polymer Resist," J. Appl. Phys., vol 56, No.4, 15 Aug. 1984.

[11] E.J. McInerney, P.A. Flinn, *IEEE/IRPS Proceedings*, 264(1982).

[12] A.K. Sinha, H.J. Levinstein, T.E. Smith, *J. Appl. Phys.* 49(4), 2423(1978).

Chapter 4

Considerations on Multilevel Interconnection Technologies

Two key process steps (thin-film patterning and planarization) in metallization technology have been discussed in the previous chapters. A new lift-off process using edge-detection (LOPED) is examined in chapter 2 as an alternative to etching for thin-film patterning. Then a non-etchback planarization process using spin-on glass (SOG) is investigated in chapter 3. It is shown that an SOG/LTO/SOG sandwich structure can result in good planarity for the following deposition. The annealed SOG film shows good electrical properties (in particular, low via-resistance) for multilevel interconnection applications. In this chapter, metallization processes will be studied from a more fundamental point of view. The aim is to identify candidate metallization processes that can be used in module fashion for many layers of metallization. Instead of solving the problems created by previous process steps (e.g. using planarization as shown in Fig.3.5), the complete metallization process is studied as one unit, and the effects of each step on the following steps are considered. A large number of process alternatives are examined, and from this comprehensive study we identify 13 generic process alternatives. Each of the 13 cases is examined in detail and examples are given to illustrate the advantages and difficulties associated with each case. Several promising metallization schemes are chosen for more detailed study.

4.1 Metallization Schemes

Multilevel-interconnection technology consists of processes for deposition and patterning of both conductive and dielectric films. Conductive films are needed as the interconnects (metal patterns) between devices and subsystems, as well as the interconnects (vias) between layers of metal films. Dielectric films are needed to separate the adjacent metal patterns, and to separate the stacked metal layers. In this section, both the conductive film and dielectric film are divided into two regions corresponding to their two functions (Fig.4.1). M1 designates

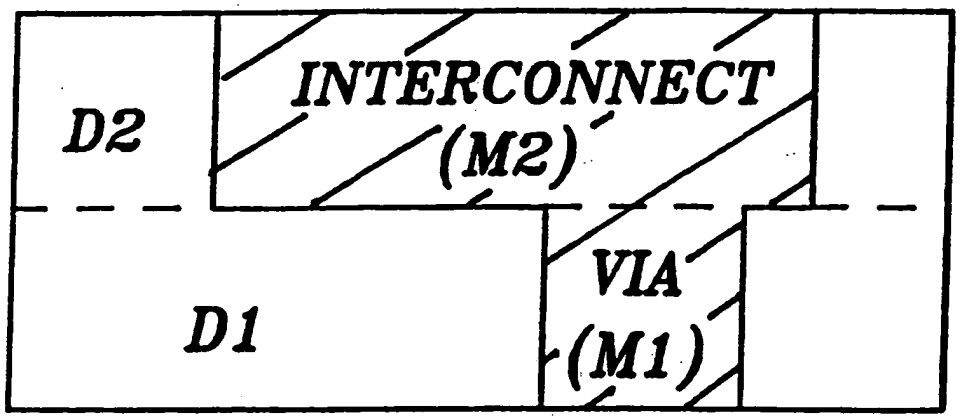


Fig.4.1 The four regions in a metallization step. M1 is the via-filling metal film, and M2 designates the metal film in the interconnect patterns. D1 is the dielectric film that embeds the vias, while D2 is the dielectric film surrounding the interconnects.

the via-filling metal film, while M2 stands for the metal film in the interconnect patterns. D1 is the dielectric film in which M1 is embedded and D2 the dielectric film surrounding M2. For any metallization process, all four regions exist, but they are generally not deposited separately. For example in the traditional metallization process, a single deposition step provides the metal filling the vias (M1) and the metal film used as the interconnect (M2). In other processes, such as the "pillar via" process as described later, the two metal films are deposited separately.

There are 24 (4!) ways to arrange the four regions (M1, M2, D1, D2). However, in reality M1 is always deposited before M2 and D1 before D2; therefore, the total number of ordering the four regions is reduced to 6 ($\frac{4!}{2!2!}$) as in Table 4.1.

Table 4.1 The 6 ways to order M1,M2,D1,D2

(1)	D1	M1	M2	D2
(2)	D1	M1	D2	M2
(3)	D1	D2	M1	M2
(4)	M1	D1	D2	M2
(5)	M1	D1	M2	D2
(6)	M1	M2	D1	D2

The first five cases will be discussed later. The sixth case (M1 M2 D1 D2) represents a metallization process in which all the metal patterns (vias and interconnects) are constructed first, and then the dielectric film is deposited (Fig.4.2). As can be seen from the figure, this process is inprobable and will not be pursued any further.

Planarization is an important issue in the discussion of the metallization process. All the planarization techniques available now (such as glass reflow, bias-sputtered quartz, or spin-on process) can only smooth the local topography rather than level the whole wafer. An isolated step several hundreds micrometers away from any other topography cannot be planarized by any existing planarization technique. It is then desirable to avoid the need for planarization if

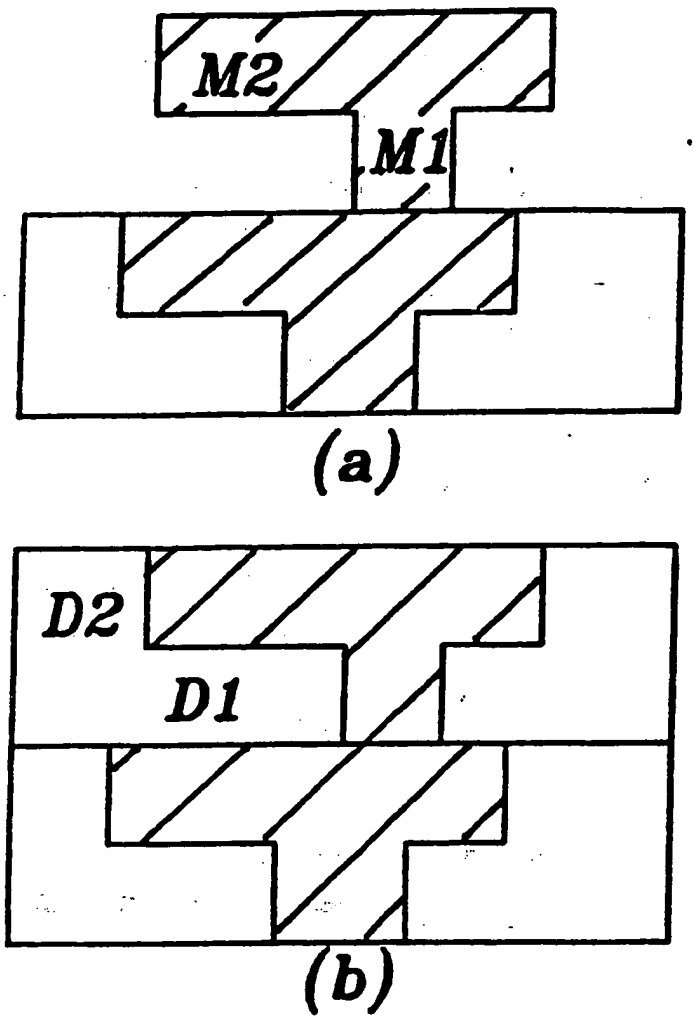


Fig.4.2 The process flow of M1 M2 D1 D2. (a) Both the vias and the interconnects are constructed first, and (b) the dielectric film (D1 & D2) are deposited and planarized. As can be seen from this figure, it is not practical to pattern the interconnect before the D1 is deposited.

possible. For each pair of metal and dielectric films (M1 D1 and M2 D2), a planarization process is generally needed if the metal film is deposited prior to the dielectric film (M1 < D1 or M2 < D2). If the dielectric film is deposited first, it is straight forward to create processes in which planarization is not needed. Assuming this assertion is true then for the five cases we will discuss later, only processes (2) and (3) belong to the class for which we can avoid the need for planarization.

The two patterning process steps, one for vias and one for metal patterns, can also be categorized according to "tone". We define bright field as a pattern process in which the feature (via or metal line) is represented by an opaque area on the mask for positive resist. Dark field is the opposite. The vias are defined by the lithography process L1 and the metal patterns by L2. If the dielectric film (D1 or D2) is deposited before the corresponding metal film (M1 or M2), the patterning process (L1 or L2) must be performed prior to the metal deposition process to create the room for the metal film. If the metal film is deposited first, the patterning process should precede the deposition of the dielectric film to remove the excess metal film. Using a self-evident notation we can summarize as follows:

$$D1 < M1 \Rightarrow L1 < M1 \quad (1a)$$

$$D2 < M2 \Rightarrow L2 < M2 \quad (1b)$$

$$M1 < D1 \Rightarrow L1 < D1 \quad (1c)$$

$$M2 < D2 \Rightarrow L2 < D2 \quad (1d)$$

In which < or > refers to time ordering, not magnitude.

Some general remarks on the metal deposition and patterning processes can also be made. If the metal deposition (M1 or M2) precedes the patterning process (L1 or L2), a blanket deposition is used to put down the metal and an etching process is used to pattern the metal film. If the patterning processes is conducted prior to the corresponding metal deposition, an additive patterning is usually used. Either the resist "guides" the deposition (e.g. electroless plating) or the resist is dissolved to selectively remove unwanted portions of the film (lift-off

). If there is another patterning process step between the patterning process and the metal deposition (e.g. L1 "L2" M1), lift-off can not be used because the patterning resist (as in L1) is usually destroyed by the following lithography process (L2).

Another important assumption made in this discussion is that the patterning material used in either L1 or L2 is not compatible with the dielectric deposition process. Although the possibility of using some high-temperature patterning materials or a low-temperature deposition process should not be excluded in a complete discussion (indeed we have demonstrated a lift-off based isolation technology using PHOTOX®[4]), these processes are not practical at present. Therefore, some combinations such as (L1 D1 M1), which requires the via patterning material to sustain the deposition process, will not be considered. The general rule is

$$\text{If } D_i < M_i \quad \text{then} \quad D_i < L_i \qquad (2)$$

Each of the five cases will be discussed in more detail in the following subsections.

4.1.1 Process (1), D1 M1 M2 D2

A common advantage of this case is that the D1 deposition of this process is immediately after the D2 deposition of the previous layer, then these two layers can be deposited by a single deposition if desired. In this case, D1 is deposited before M1; therefore, L1 should precede M1 as required by (1a). From (2), L1 cannot be the first step; consequently, the order for via-related process is D1 L1 M1. L1 in this case is the via-opening process (i.e. dark field lithography and dielectric etching). Since M2 is deposited prior to D2, (1d) requires that L2 be completed before D2 deposition. There are five potential choices for locating L2 as labeled by (i) to (v) below:

L2 prior to (i) D1 (ii) L1 (iii) M1 (iv) M2 (v) D2

Order (i) is not allowed for the same reason that derives requirement (2) in the last section. Order (ii) is also not practical unless L1 and L2 use different material for patterning; otherwise, the L1 process will remove the L2 material (i.e. photoresist). Order (iii) to (v) will be dis-

cussed in detail with their cross-sections.

(A) D1 L1 L2 M1 M2 D2.

After the completion of the previous metallization process, a dielectric film (D1) is deposited to the thickness of the desired inter-layer dielectric film thickness (Fig.4.3(a)). The dark-field via mask is used in lithography and an etching step opens the via to the underlying metal patterns, followed by a resist-stripping process (Fig.4.3(b)). Another lithography step (L2) generates the metal patterns on the substrate (Fig.4.3(c)). A dark-field metal mask, on which the metal patterns are transparent, is used since the metal film is yet to be deposited into the pattern areas. Now the substrate is ready for the metal deposition (M1 and M2). One way to deposit the metal film is using a blanket deposition all over the substrate for both M1 and M2 (Fig.4.3(d)). Then a lift-off process can remove the L2 photoresist and the excess film on top of it, leaving the filled vias and metal patterns (Fig.4.3(e)). A second dielectric film deposition and a planarization process are needed to complete the process (Fig.4.3(f)). An alternative way to deposit the metal films is to put down M1 first, then M2 by another deposition. A lift-off process cannot be used to pattern M1 because the L1 resist does not exist in this step. Low-temperature selective deposition, such as electroless plating, can fill the via (Fig. 4.3(d')), and a selective deposition or a lift-off process can put down M2 (Fig.4.3(e')). Similarly, a deposition and a planarization process are needed for D2 (Fig.4.3(f)).

The process using a blanket deposition for both M1 and M2 (Fig.4.3a,b,c,d,e,f) is the lift-off process described in chapter 2 and in other lift-off papers[1-5]. The step coverage of the metal deposited into the via is one of the key limiting factors for this process. An aspect ratio over one (e.g. $\frac{\text{1.0μm resist + 0.6μm dielectric}}{\text{1.0μm wide via}} = 1.6$) is easily encountered in today's microelectronics process. Tapered sidewalls of the resist or of the vias can help the step coverage with additional complexity to the process. The other process (Fig.4.3a,b,c d',e',f) is a combination of a selective via-filling process and an additive thin-film patterning process for

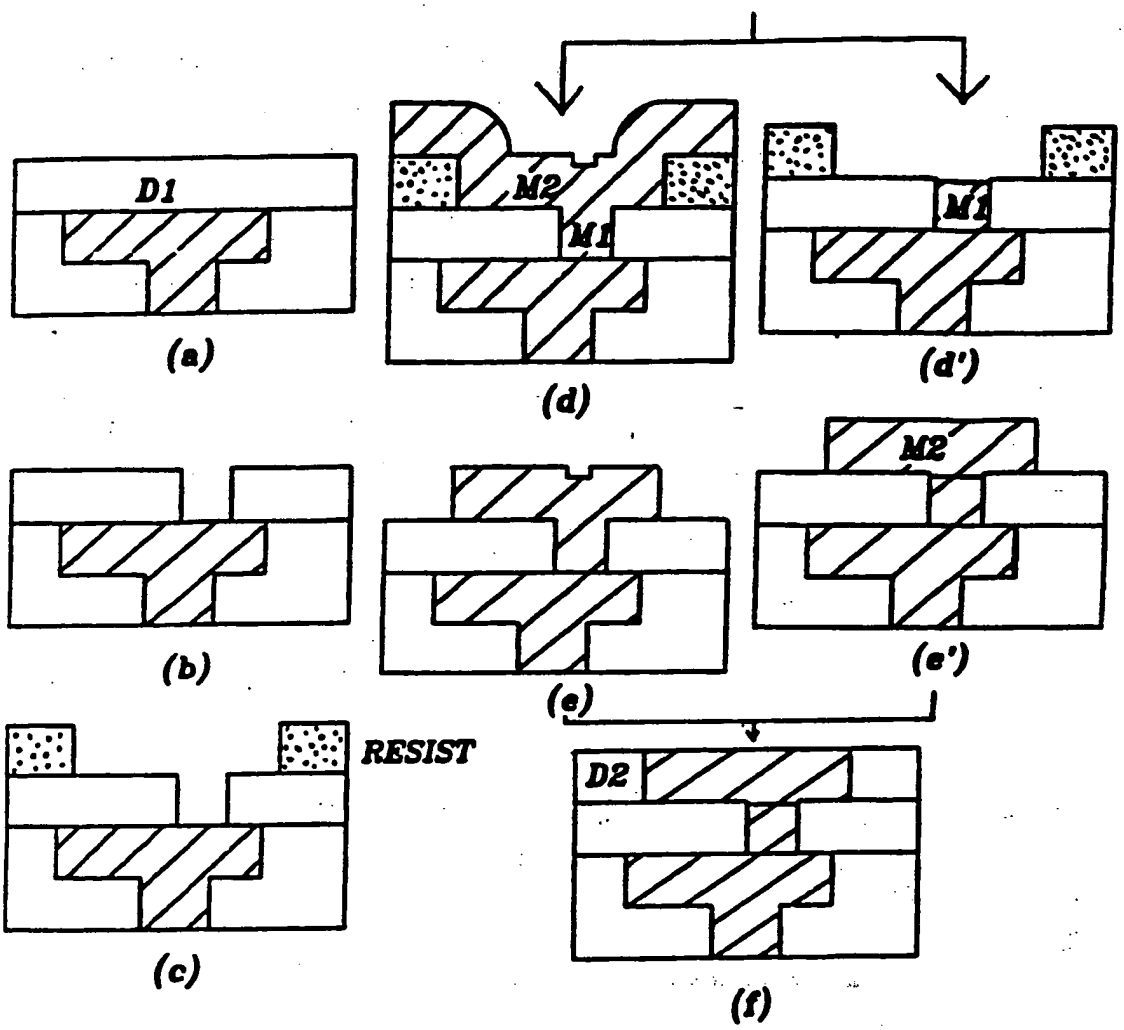


Fig.4.3 The process flow of the D1 L1 L2 M1 M2 D2 sequence. (a) A dielectric film (D1) is deposited to the thickness of the desired inter-layer dielectric film thickness first. (b) Then the dark-field via mask is used in lithography and an etching step opens the via to the underlying metal patterns (L1), followed by a resist stripping process. (c) Another lithography step (L2) generates the dark-field metal patterns on the substrate. (d) A blanket deposition all over the substrate is used for both M1 and M2. (e) Then a lift-off process can remove the L2 photoresist and the excess film on top of it, leaving the filled vias and metal patterns. (f) A second dielectric deposition (for D2) and a planarization process are needed to complete the process. (d') An alternative way to deposit the metal films is to put down M1 selectively first, (e') and a selective deposition or a lift-off process can deposit M2. The process is completed by depositing D2 and planarizing the topography.

metal patterns, and provides better step coverage in the via than the first one. Both processes require a planarization process for D2 if a reasonably flat topography is to result. Even with a planarization step (such as bias sputtered SiO_2 deposition) the topography generated in this step (equal to the thickness of M2) will accumulate as more and more layers are added.

(B) D1 L1 M1 L2 M2 D2

In this case, the L2 patterning process separates the two metal deposition processes. The first two steps (Fig.4.4(a) and (b)) are similar to the previous case, except that the L1 resist is not necessarily removed. If a lift-off process is used for M1, the L1 resist can serve as the lifting medium. If M1 is deposited selectively, the resist may be removed after the vias are opened. After the M1 deposition (Fig.4.4(c)), a second lithography step using a dark-field metal mask patterns the L2 resist on the substrate (Fig.4.4 (d)). Either a selective deposition or a lift-off process can be used for M2 (Fig.4.4(e)). The process is completed by the D2 deposition and a planarization step (Fig.4.4(f)).

The via filling part of this process is reasonably planar; however the metal pattern results in an unfavorable topography. Planarization is essential, and as in the previous case the problem of accumulated topography remains.

(C) D1 L1 M1 M2 L2 D2

The first two steps in this case are similar to those in the first two cases (Fig.4.5(a) and (b)). The L1 resist must be removed if a blanket deposition is used for both M1 and M2 (Fig.4.5(c)). If a lift-off process or a selective deposition is used for M1 (Fig.4.5(c')), the L1 resist can either be used as a lifting medium or be removed. A blanket deposition of M2 is needed because L2 follows M2 (Fig.4.5(d)). The M2 film is patterned by a bright-field metal mask and an etching step (Fig.4.5(e)). The dielectric film D2 is then deposited and planarized (Fig.4.5(f)).

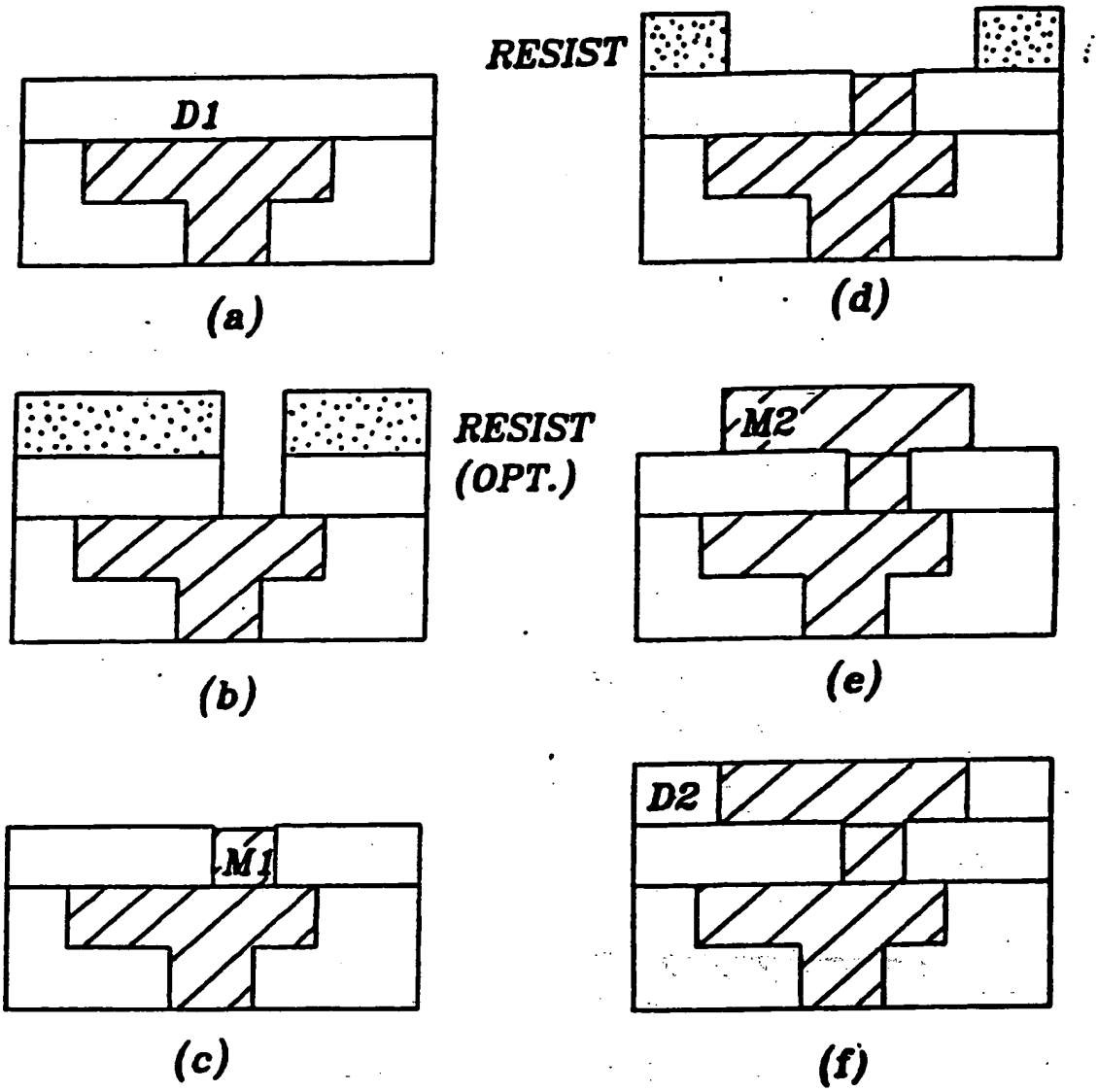


Fig.4.4 The process flow for D1 L1 M1 L2 M2 D2. (a) A thick dielectric is deposited first, (b) followed by the dark-field via lithography. (c) M1 is then deposited either by selective deposition or by lift-off. (d) A second lithography step using a dark-field metal mask patterns the L2 resists on the substrate. (e) Either a selective deposition or a lift-off process can be used for M2. (f) The process is completed by the D2 deposition and a planarization step.

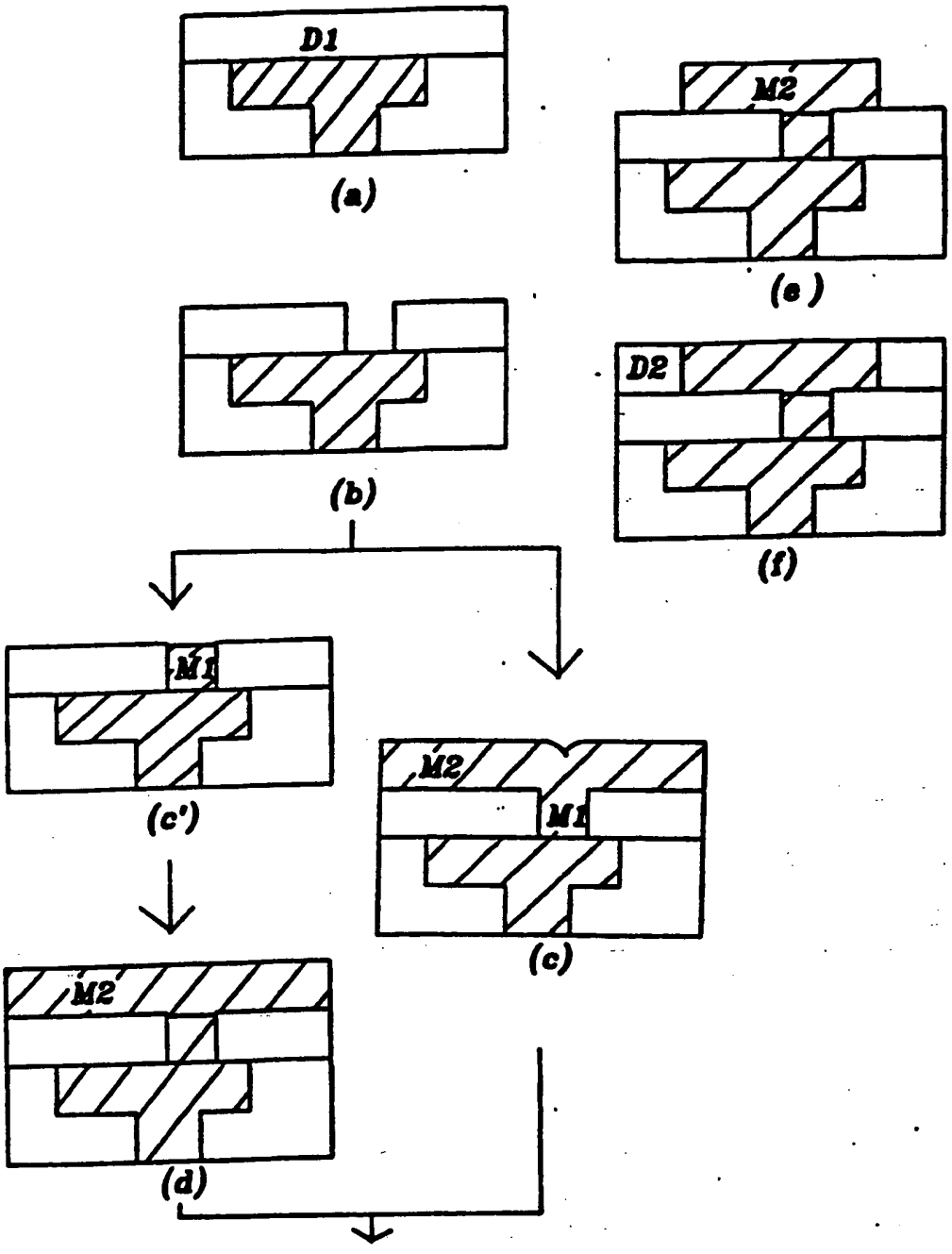


Fig.4.5 The process flow for D1 L1 M1 M2 L2 D2. (a) A thick dielectric film is deposited on the substrate as D1. (b) The dark-field via lithography generate the via patterns on the oxide. (c) A blanket deposition is used to deposit both M1 and M2. (c') An alternative process is to deposit M1 first, then (d) M2 by a blanket deposition. (e) The bright-field metal mask is used to pattern the m2 film. (f) Finally the dielectric film d2 is deposited and planarized.

The blanket deposition process (Fig.4.5a,b,c,e,f) is the traditional metallization process and covers most reported metallization processes [6-8]. The other process (Fig.4.5a,b,c',d,e,f) is also proposed by some authors, and usually the via-filling processes are stressed in their reports [9-11]. As in the previous case , planarization of the dielectric D2 is still needed, and topography still accumulates over metal layers. None of the variations on process (1) can provide a truly planar topography.

4.1.2 Process (2), D1 M1 D2 M2

In this case, D1 is deposited before M1; thus L1 should be completed before M1 (1a). Similarly L2 should precede M2 because M2 is deposited after D2 (1b). Also from (2), L1 must be carried out after D1 and L2 after D2. As a result, there is only one way to insert L1 and L2 into the array:

D1 L1 M1 D2 L2 M2

The first two steps in this case are similar to the previously discussed cases. A layer of dielectric film is deposited (Fig.4.6(a)) and vias are opened (Fig.4.6(b)). The M1 can be deposited either by a lift-off process or by a selective deposition process (Fig.4.6(c)). The process is repeated for the D2 L2 M2 sequence (Fig.4.6(d)-(f)). The etching step in Fig.4.6(e) should have high selectivity so that D2 can be completely etched while D1 remains intact. An "etch stop" of a different material from D1 and D2 can be deposited after D1 and before D2 deposition.

This process has not been widely examined yet, but the inherent planarization from the buried metal films is very attractive for the multilevel interconnection technology. If a good selective deposition process is available, this process deserves more attention in the future. If the lift-off process is used for metal patterning, the step coverage, especially for M1, must be carefully examined first. The separate depositions for D1 and D2, as well as for M1 and M2, add to the process complexity; however the minimal need for planarization potentially

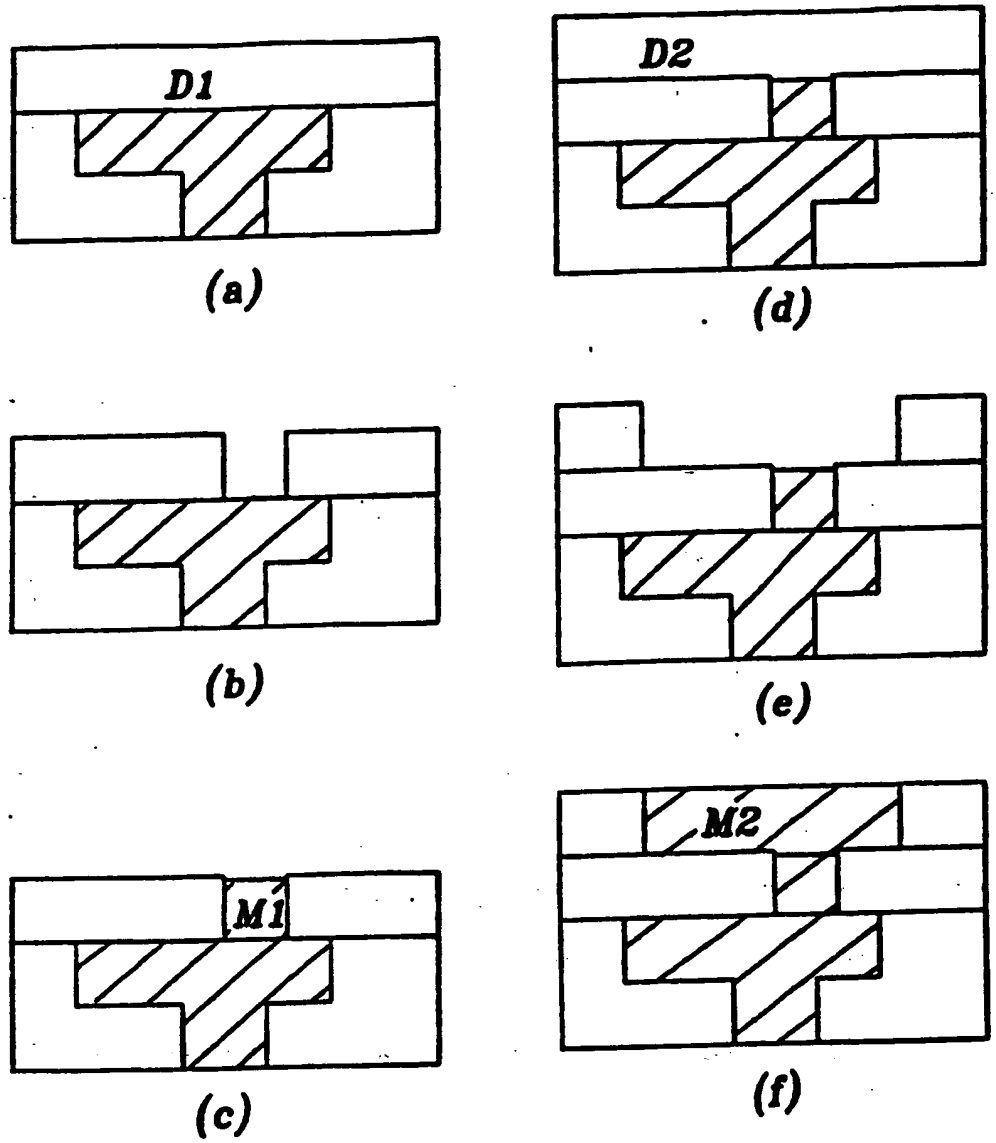


Fig.4.6 The process flow for D1 L1 M1 D2 L2 M2. (a) A thick dielectric film is deposited as D1. (b) The dark-field vias mask is used to generate the via patterns on the dielectric. (c) M1 is deposited selectively or by lift-off. (d) Another dielectric film is deposited as D2, (e) followed by the dark-field metal mask for L2. (f) The process is completed by depositing M2 into the L2 patterns by selective deposition or lift-off.

outweighs this disadvantage.

4.1.3 Process (3), D1 D2 M1 M2

In this case, D1 is deposited before M1, and therefore, from (1a) L1 should precede M1. From (2) the L1 process should be after the deposition of both D1 and D2. As a result, the only location to insert L1 is between D2 and M1. Similarly, L2 must come after D2 and before M2. There are three locations to insert L2 prior to:

(i) L1 (ii) M1 (iii) M2

These three cases will be discussed individually. The fact that D2 is immediately after D1 suggests that D1 and D2 can be deposited in a single step. Both D1 and D2 are deposited before M1 and M2; thus, in principle no planarization process is needed for either dielectric film. All the three approaches require a dielectric etch to pattern D2 without etching D1. An intermediate layer deposited before D2 can serve as the "etch stop".

(A) D1 D2 L2 L1 M1 M2

A thick dielectric film (to the sum of the interlayer dielectric film thickness and the metal film thickness) is deposited first (Fig.4.7(a)). A dark-field metal mask is used in L2 and the patterns are transferred into D2 by an etching step (Fig.4.7(b)). Then the photoresist is removed, and another layer of photoresist is applied for L1. The dark-field via mask is used in L1 and the vias are opened through D1 to the underlying metal patterns (Fig.4.7(c)). The vias are filled either by a selective deposition or lift-off, and after that the L1 resist is stripped (Fig.4.7(d)). M2 is deposited by a selective deposition method as in Fig.4.7(e).

This process has not been widely studied yet [12]. The planarized surface after processing makes this process very attractive as the building block for multi-level metallization process. For the M1 deposition, selective deposition is preferred to lift-off due to the high aspect ratio in this case (e.g. $\frac{1.0\mu m \text{ resist} + 0.8\mu m \text{ metal thickness} + 0.6\mu m \text{ dielectric}}{1.0\mu m \text{ wide via}} = 2.4$). M2

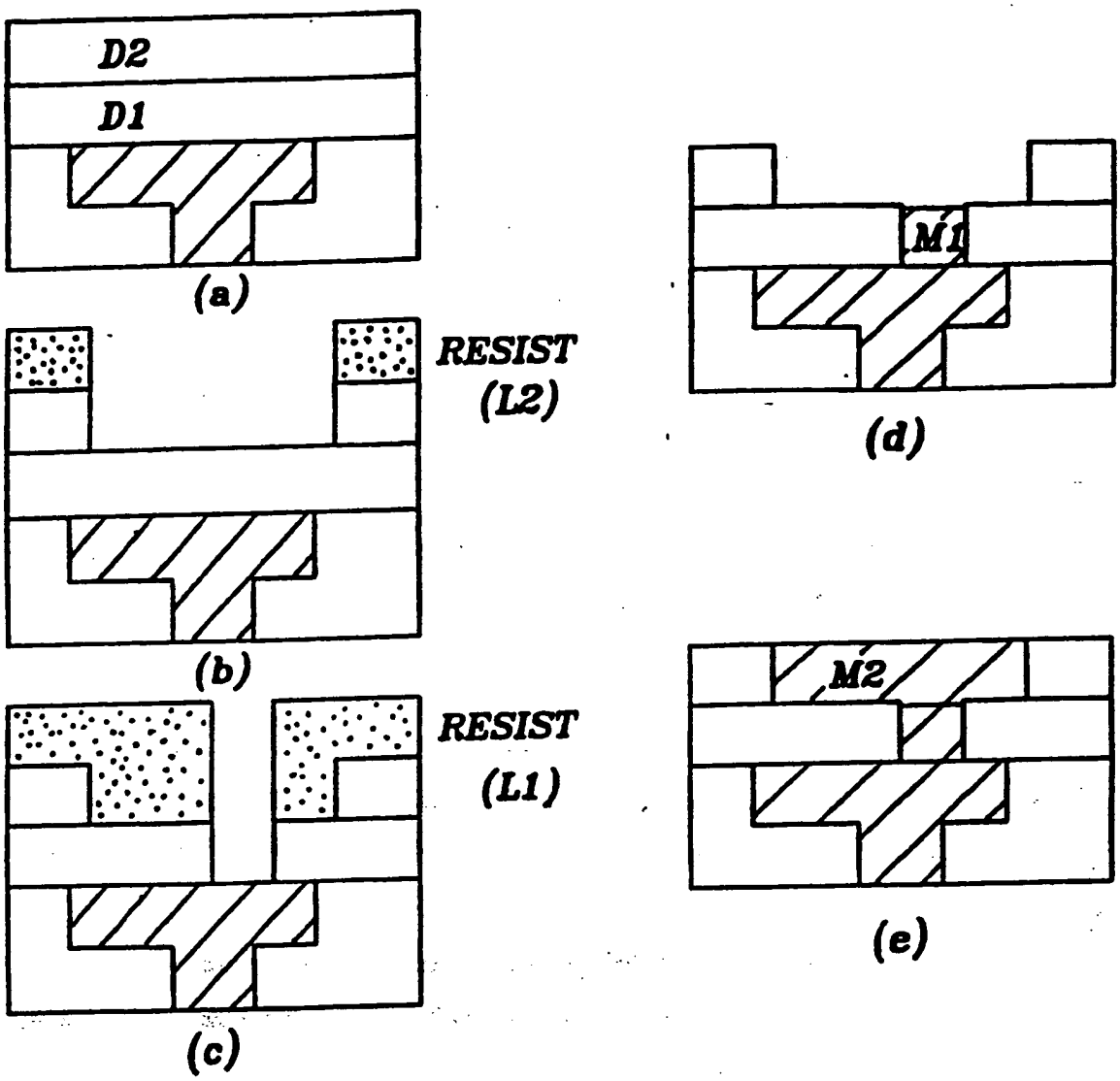


Fig.4.7 The process flow for D1 D2 L2 L1 M1 M2. (a) A thick dielectric film (D1 and D2) is deposited first. (b) A dark-field metal mask is used in L2 and the patterns are transferred into D2 by an etching step. (c) The dark-field via mask is used in L1 and the vias are opened through D1 to the underlying metal . (d) The vias are filled either by a selective deposition or lift-off, and after that the L1 resist is stripped. (e) M2 is then deposited by a selective deposition process.

can only be deposited by a selective deposition process since the L1 process removes the L2 resist. However selective deposition may not be easy to achieve, especially if D1 and D2 are the same material. (In principal a nucleating agent could be deposited after the L2 step, prior to resist removal.)

(B) D1 D2 L1 L2 M1 M2

In this case, a thick dielectric film is deposited as D1 and D2 (Fig.4.8(a)). Then a photolithography step using the dark-field via mask, together with an etching step, transfers the pattern through both D1 and D2. After the L1 resist is removed (Fig.4.8(b)), another lithography step using dark-field metal mask and an etching step are used to pattern D2 (Fig.4.8(c)). One way to deposit M1 and M2 is to use two separate metal depositions. M1 can be deposited by a selective deposition as in Fig.4.8(d). Lift-off cannot be used for M1 since L2 is between L1 and M1. Then M2 can be deposited either by a selective deposition or a lift-off process (Fig.4.8(e)). M1 and M2 can also be deposited with one deposition and patterned by a lift-off process (Fig.4.8(e)).

If the etching selectivity ($= \frac{\text{the etch rate of dielectric}}{\text{the etch rate of metal}}$) is not high enough, D1 can be partially etched in the L1 patterning step and completely etched in the next step (L2). Both processes (Fig.4.8a,b,c,d,e and Fig.4.8a,b,c,e) provide good planarity and are good candidates for future interconnection technology. In the process using the blanket deposition and lift-off, the step coverage in the via may be a concern. The selective deposition process is preferred in this case. This case is similar to the previous after step (c) if the L2 resist is removed. However, by retaining this resist it is possible to easily deposit or implant a nucleation layer for the selective deposition of M2. Thus the ordering L1 L2 seems to have an advantage over L2 L1.

(C) D1 D2 L1 M1 L2 M2

A thick dielectric film (D1 and D2) is deposited first as in Fig.4.9(a). A photolithography step using the dark-field via mask and an etching step are needed in L1 to open the

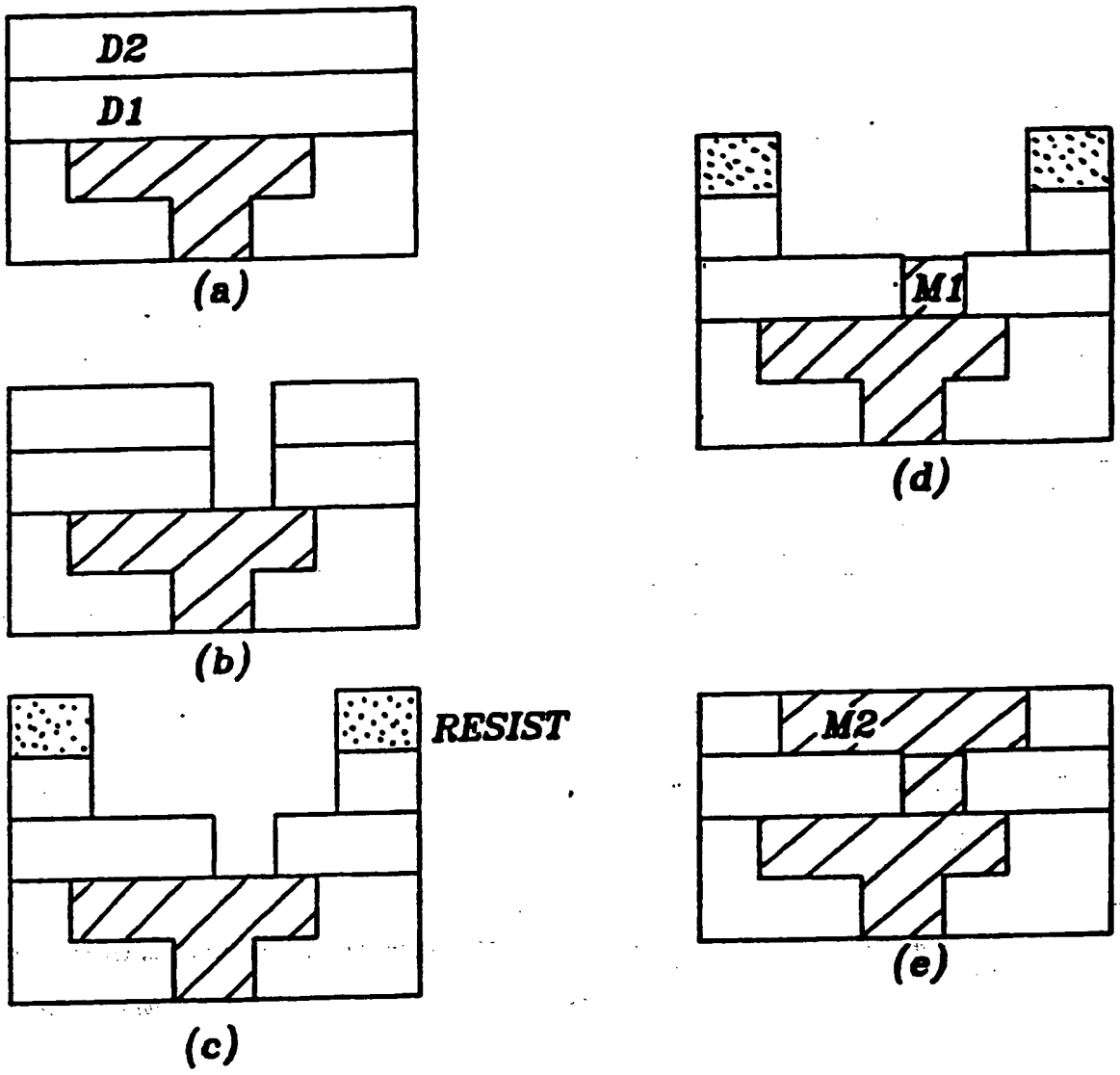


Fig.4.8 The process flow for D1 D2 L1 L2 M1 M2. (a) A thick dielectric film is deposited. (b) The dark-field via mask is used in a lithography step, and an etching step transfers the patterns through D1 and D2. (c) A lithography step using the dark-field metal mask and an etching step pattern D1. (d) M1 is deposited by selective deposition. (e) M2 is deposited by selective deposition or lift-off.

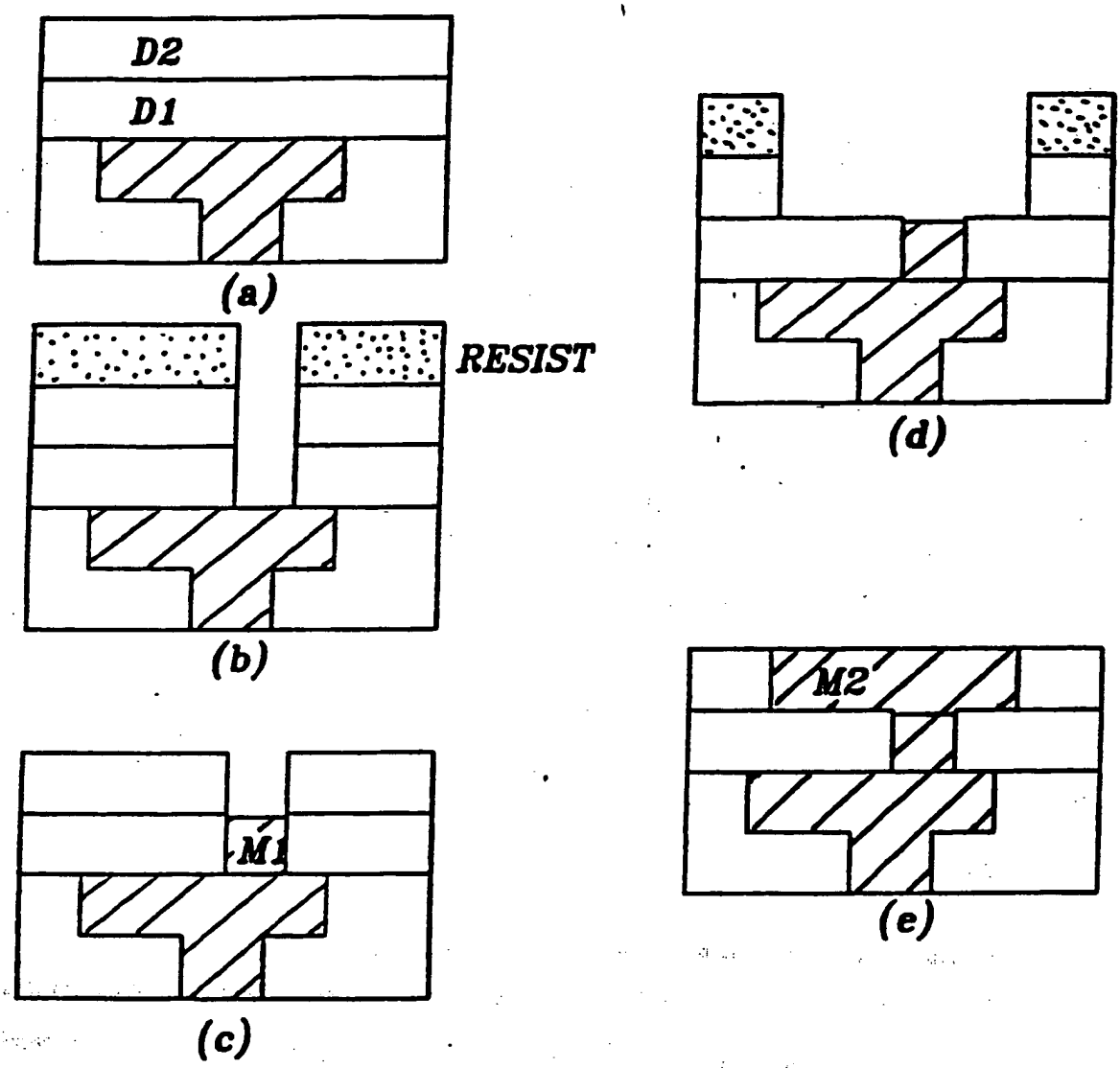


Fig.4.9 The process flow for D1 D2 L1 M1 L2 M2. (a) A thick dielectric film is deposited. (b) A lithography step using dark-field via mask and an etching step are used to pattern both D1 and D2. (c) M1 is deposited by selective deposition or lift-off. (d) D1 is patterned by a dark-field metal mask and an etching process. (e) M2 is deposited by selective deposition or lift-off.

dielectric film to the underlying metal patterns (Fig.4.9(b)). M1 is deposited in this case either by a selective deposition or by a lift-off process (Fig.4.9(c)). Another lithography step using the dark-field metal mask and an etching step are used in L2 to pattern D2 (Fig.4.9(d)). M2 can also be deposited selectively or by lift-off (Fig.4.9(e)).

This case is similar to the two previous cases. However the metal M1 must be deposited deep with a high-aspect hole. Selective deposition for M1 is preferred to lift-off due to the high aspect ratio. The process also results in good planarity without the requirement of any planarization process.

4.1.4 Process (4), M1 D1 D2 M2

In this case, M1 is deposited before D1, and thus L1 must be completed before the D1 deposition (1c). The L1 step can be inserted either before M1 deposition or after M1 deposition (L1 M1 D1 or M1 L1 D1). D2 comes before M2, so the L2 step should be prior to M2 (1b). From (2), we also know that L2 should be after D2. Thus, there are only two possible ways to order the process steps in this case:

L1 M1 D1 D2 L2 M2

M1 L1 D1 D2 L2 M2

In both cases M1 is pattered before D1 deposition, and the processes are usually called the "pillar" technology [13-14]. The advantage is a better step coverage for the via compared to a single metal deposition approach [13,14]. The two dielectric film, D1 and D2, are not separated by any other step, and can be deposited in a single step. However if a truly planar topography is desired , the dielctric must somehow be planarized. For sufficiently small vias fill planarization is possible by a number of technologies, including bias-sputtered quartz. Both approaches pattern D2 by a dielectric etch, which should not attack the underlying D1. An intermediate layer is needed as the "etch stop". If the vias are patterned by etching, the underlying metal

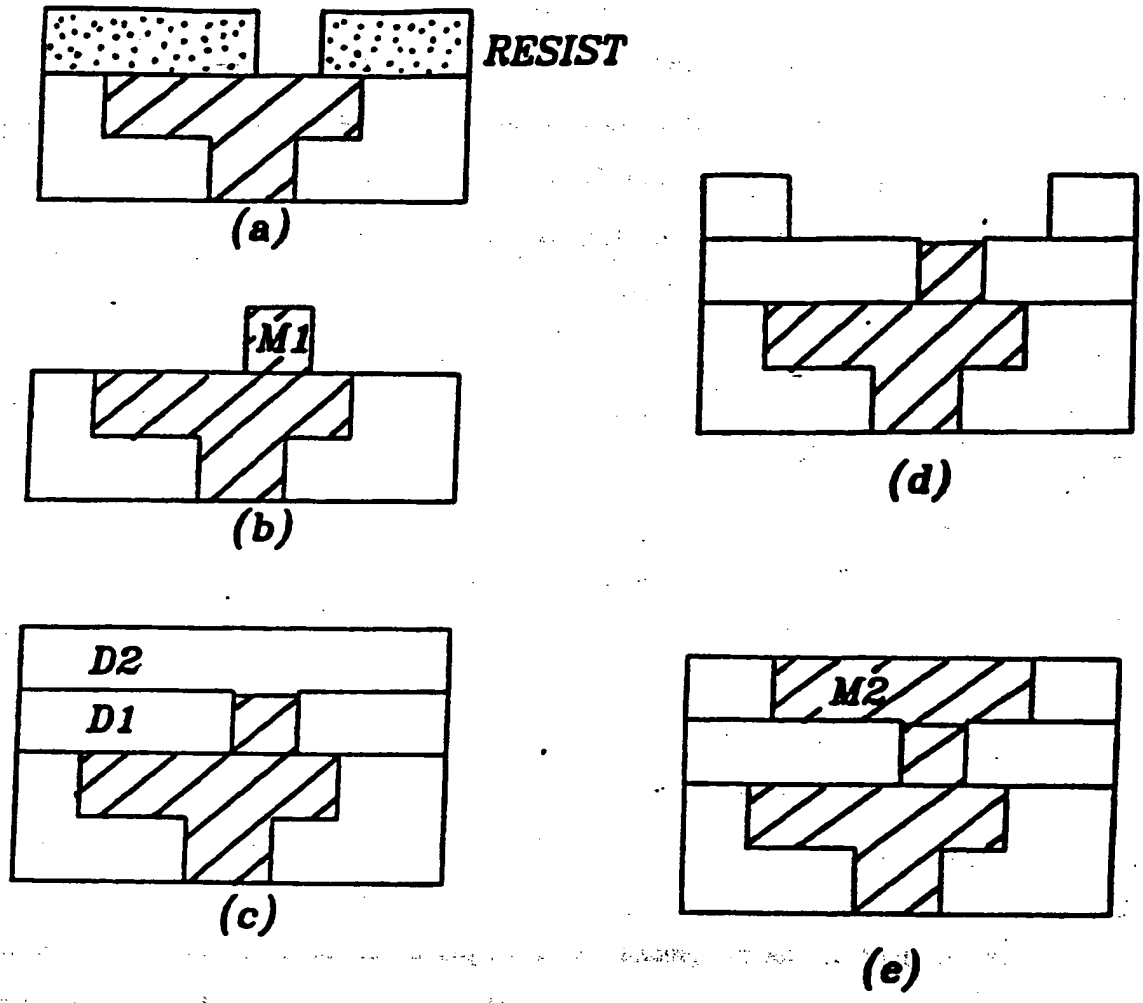


Fig.4.10 The process flow for L1 M1 D1 D2 L2 M2. (a) First a layer of photoresist is patterned by a dark-field via mask. (b) Then M1 is deposited either by selective deposition or by lift-off, followed by the resist removal process. (c) A single deposition with the necessary planarization puts down both the D1 and D2. (d) The dark-field metal mask is used in L2 lithography and an etching step transfers the patterns through D2. (e) M2 is also deposited either by selective deposition or by lift-off.

patterns should not be attacked. It is also recommended to deposit a barrier layer after the previous M2 layer as the "etch stop". *(A) L1 M1 D1 D2 L2 M2*

First a layer of photoresist is patterned by a dark-field via mask (Fig.4.10(a)), and then M1 is deposited either by selective deposition or by lift-off, followed by the resist removal process (Fig.4.10(b)). A single deposition with the necessary planarization puts down both D1 and D2 (Fig.4.10(c)). The dark-field metal mask is used in L2 lithography and an etching step transfers the patterns through D2 (Fig.4.10(d)). M2 is also deposited either by selective deposition or by lift-off (Fig.4.10(e)).

The first part of the process uses additive patterning to form the pillars. The deposition of M2 is just the "buried" metal process already discussed [12,15-16]. In this process D1 needs to be planarized instead of D2 and can be a potential problem when several layers of metal are needed. The planarization of D1 is easier than D2 because in most cases vias have only one size, and a specific planarization process (such as bias-sputtered quartz) can be designed to take care of this problem.

(B) M1 L1 D1 D2 L2 M2

This case differs from the previous one only in the sequence of forming the via-pillars; in this case a simple deposition and etching forms the vias. It has been reported by several authors under various names such as "pillar" or "stud" [13,14]. All other comments from the last case hold true for this process. A further possible complication arises to the need for selectivity in etching M1; different metals would be preferred such that M2 has a low etch rate in the etchant for M1.

4.1.5 Process (5), M1 D1 M2 D2

This is the last case being discussed. M1 is deposited before D1, thus L1 before D1. Similarly the fact that M2 is before D2 leads to L2 before D2. Each patterning process (L1

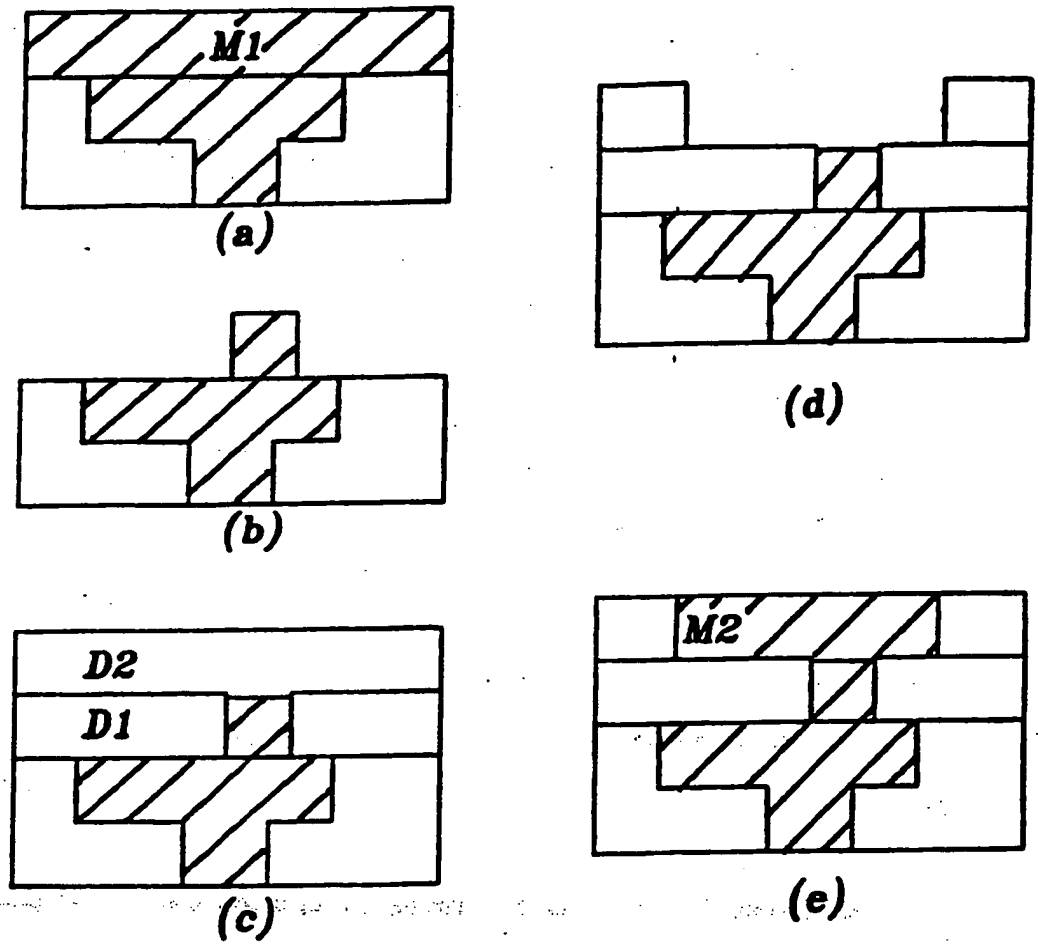


Fig.4.11 The process flow for M1 L1 D1 D2 L2 M2. (a) M1 is deposited by a blanket deposition first. (b) The bright-field via mask and a metal etching step pattern the film. (c) A single deposition with planarization is used for D1 and D2. (d) L2 uses a dark-field metal mask and an etching process to pattern D2. (e) M2 is deposited by an additive patterning process.

or L2) can be either before the metal deposition (L1 M1 or L2 M2) or after it (M1 L1 or M2 L2). There are in total four cases to study:

L1 M1 D1 L2 M2 D2

M1 L1 D1 L2 M2 D2

L1 M1 D1 M2 L2 D2

M1 L1 D1 M2 l2 D2

A careful examination of these four cases reveals that there are actually two processes, LMD and MLD, for the two regions (1 and 2). We will examine these two basic processes instead of the four individual cases.

The LMD process is shown in Fig.4.12. A layer of resist is patterned by the dark-field mask (Fig.4.12(a)), followed by the deposition of the metal film using selective deposition or lift-off (Fig.4.12(b)). Then the dielectric film is deposited with the needed planarization process (Fig.4.12(c)). The MLD process puts down the metal film first (Fig.4.13(a)), and then the bright-field mask lithography and the etching step pattern the metal film (Fig.4.13(b)). The dielectric film is deposited and planarized (Fig.4.13(c)).

The M1 L1 D1 M2 L2 D2 process is the standard pillar process reported by Sirkin [13] and Welch [14]. All the other processes are just variations of the pillar process by replacing one or both of the subtractive metal patterning to an additive process. All the four processes require planarization for both D1 and D2. The topography is severe and the complexity high as the the number of metallization layers increases. If the MLD process is used for the via patterning, a buffer layer is needed after the previous L2 layer is deposited.

4.1.6 Comparisons of the Metallization Schemes

All the 13 cases discussed before are compared in Table 4.2. Planarization is one of the key indicators in this comparison because a process requiring planarization cannot be used to construct a metallization process with more than three or four layers of metal films. The deposition methods for both M1 and M2 are also listed in this table.

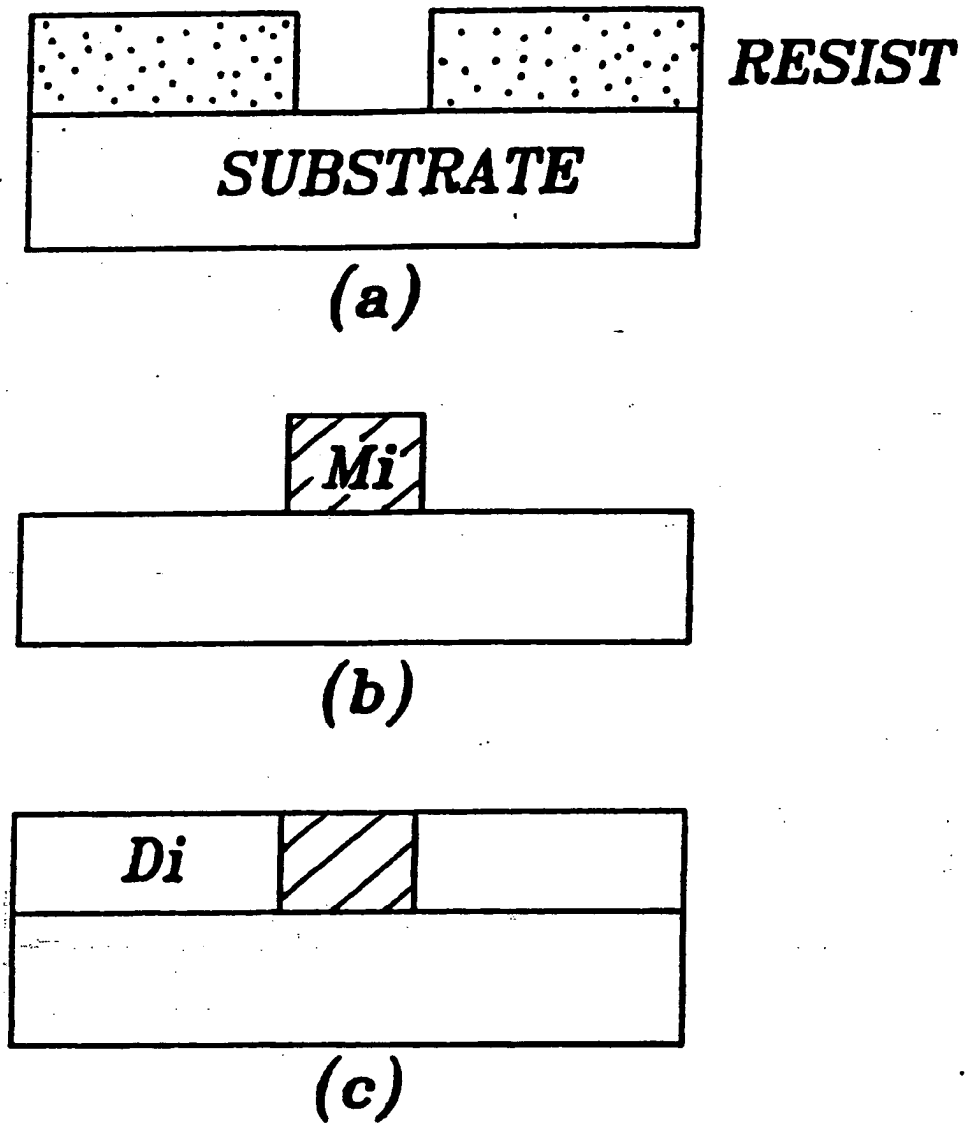


Fig.4.12 The process flow for L M D. (a) A layer of resist is patterned by the dark-field mask. (b) The metal is deposited by selective deposition or lift-off. (c) The dielectric film is deposited with the needed planarization process.

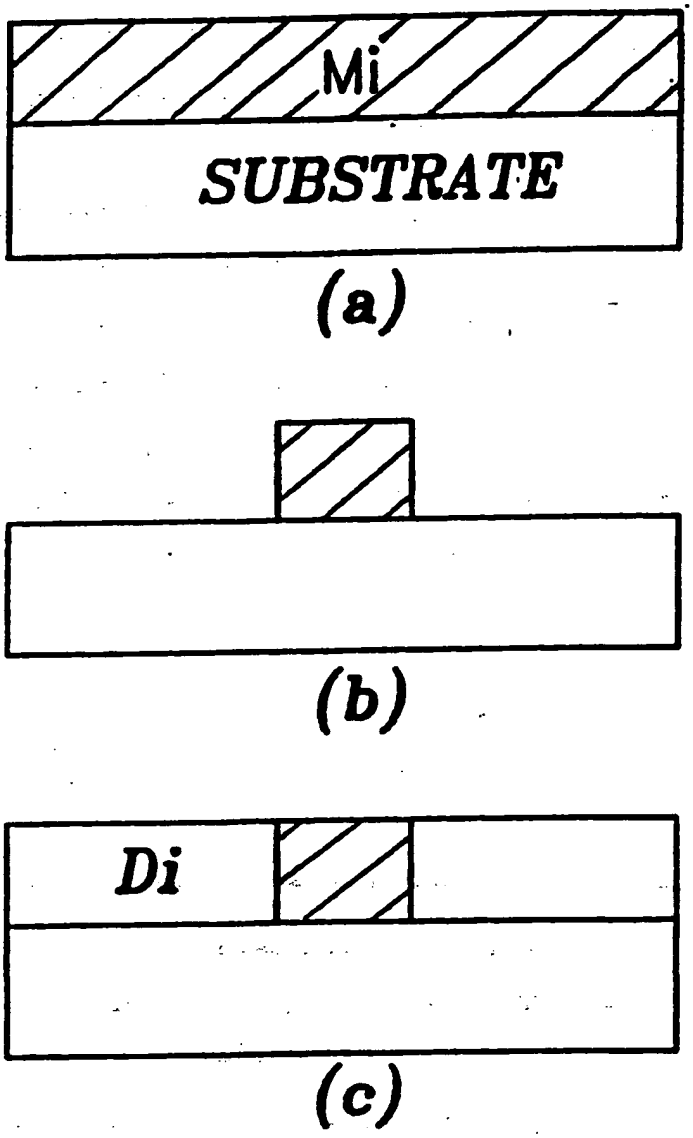


Fig.4.13 The process flow for M L D. (a) The metal film is deposited by a blanket deposition. (b) The bright-field mask lithography and the etching step pattern the metal film (c) The dielectric film is deposited and planarized.

As can be seen from the table, there are only four cases (Fig.4.6 to Fig.4.9) that do not require any form of planarization. The cases of Fig.4.10 and 4.11 are almost as attractive since D1 planarization is more easily accomodated. They will be discussed in more detail in section 4.4.

Table 4.2 Comparison of the 13 Cases

Fig.	Possible Permutations	M1 deposited by	M2 deposited by	Comments
4.3	D1 L1 L2 M1 M2 D2	Blanket or Selective	Selective or Lift-Off	B
4.4	D1 L1 M1 L2 M2 D2	Selective or Lift-Off	Selective or Lift-Off	B
4.5	D1 L1 M1 M2 L2 D2	Blanket	Blanket	B
4.6	D1 L1 M1 D2 L2 M2	Selective or Lift-Off	Selective or Lift-Off	C
4.7	D1 D2 L2 L1 M1 M2	Selective or Lift-Off	Selective	C,E
4.8	D1 D2 L1 L2 M1 M2	Selective	Selective or Lift-Off	C
4.9	D1 D2 L1 M1 L2 M2	Selective or Lift-Off	Selective or Lift-Off	C,E
4.10	L1 M1 D1 D2 L2 M2	Selective or Lift-Off	Selective or Lift-Off	A,C
4.11	M1 L1 D1 D2 L2 M2	Blanket	Selective or Lift-Off	A,C,D
4.12	L1 M1 D1 L2 M2 D2	Selective or Lift-Off	Selective or Lift-Off	A,B
4.12&13	M1 L1 D1 L2 M2 D2	Blanket	Selective or Lift-Off	A,B,D
4.12&13	L1 M1 D1 M2 L2 D2	Selective or Lift-Off	Blanket	A,B
4.13	M1 L1 D1 M2 L2 D2	Blanket	Blanket	A,B,D

Comments. A: D1 needs planarization. B: D2 needs planarization. C: Selective dielectric etch is required. D: Selective metal etch is required. E: Exceedingly high aspect ratio for via filling.

For most cases that do not require planarization, a selective deposition or a lift-off process is needed for metal deposition. The lift-off approach requires a directional deposition for metal film. Evaporation can be used for most applications except the M1 deposition in Fig.4.7 and Fig.4.9, in which the aspect ratios are exceedingly high. A discussion of one possible

selective deposition method, namely electroless plating, is given in the next section with the emphasis on the applications in the multilevel interconnection technology.

4.2 Electroless Plating as a Selective Deposition Process

Selective deposition puts down the desired film onto a specific areas, but not onto other areas. Examples of selective deposition processes are selective tungsten and electroless plating. The selective tungsten process is under intensive commercial development. It is reviewed in section 2.1 and will not be repeated here. The electroless plating of Pd, Ni, Cu and Au will be discussed in this section as alternative selective deposition processes.

The chemical vapor deposition (CVD) process deposits the desired film from a gaseous source at a temperature usually higher than 250°C; the electroless plating process deposits the desired metal film from aqueous solution at a temperature typically between 0°C and 100°C. The plating solution consists mainly of the desired metal ions, reducing agents (e.g. dimethylamine borane) and buffer chemicals. The electroless plating process can be summarized by the following reactions [17]:

$$RH \rightarrow R + H \quad (3)$$

$$R + OH^- \rightarrow ROH + e^- \quad (4)$$

$$H + H \rightarrow H_2 \quad (5)$$

$$H + OH^- \rightarrow H_2O + e^- \quad (6)$$

$$M^{n+} + ne^- \rightarrow M \quad (7)$$

Where RH represents the reductants. The electrochemical requirements for deposition are, first, the oxidation potential of the reductant's (reaction (4)) is more negative than the reversible potential of the metal to be deposited (reaction (7)); second, the metal has enough catalytic activity for the anodic oxidation to take place at a reasonable rate. The second requirement can be met by varying the PH values and the temperature of the solution. The first requirement can be discussed with the potential (E^*) for the anodic oxidation of reductants on different metals in Table 4.3 [17].

The reversible potential of metals in the complex solutions used in the electroless plating processes are usually in the range from -0.65V to -0.45V (SCE) [18]. Any potentials in Table 4.3 more negative than -0.65V indicate the solutions are available for the metal deposition. Ni and Pd can be deposited in most solutions except HCHO. Cu can be deposited at the highest rate in HCHO (most negative E*). $NaBH_4$ can be used to deposit all the metals listed.

Table 4.3 The Potentials (E*) for the Anodic Oxidation of Reductants on Different Metals at $1.0\times10^{-4}A/cm^2$.

Reductants	Metal	E* (vs. SCE)
NaH_2PO_2	Au	-0.982
	Ni	-0.935
	Pd	-0.910
	Co	-0.854
	Pt	-0.300
HCHO	Cu	-0.906
	Au	-0.770
	Ag	-0.675
	Pt	-0.508
	Pd	-0.464
	Ni	0.366
	Co	0.450
$NaBH_4$	Ni	-1.190
	Co	-1.180
	Pd	-1.136
	Pt	-0.983
	Au	-0.850
	Ag	-0.832
	Cu	-0.761
DMBA*	Ni	-0.866
	Co	-0.832
	Pd	-0.766
	Au	-0.650
	Pt	-0.633
	Ag	-0.565
NH_2NH_2	Co	-0.940
	Ni	-0.871
	Pt	-0.800
	Pd	-0.797
	Cu	-0.556
	Ag	-0.460
	Au	-0.413

* Dimethylamine borane

In most applications, the areas to be deposited on usually go through an activation process, in which a catalytic film is deposited on the surface first. Pd is the most widely used material in the activation step. The electroless plating processes for Pd, Ni, Cu and Au, together with their applications in the interconnection technology will be discussed briefly.

Pd deposition is needed in most activation steps and the process can be extended to fill the vias, but the resistivity of Pd (ρ_{Pd} = 10.8μΩ–cm) is too high to be used as the main interconnect layer. Electroless-plated Ni has been proposed to fill the vias [10]. Ni requires Pd activation and also has a relatively high resistivity (ρ_{Ni} = 6.84μΩ–cm). Both materials are attractive in via filling (for a 1μm deep and 1μm square vias, R_{via} = 0.11Ω for Pd and 0.07 Ω for Ni) and neither process attacks photoresist (PH < 11 for both cases).

Cu is extremely attractive as an alternative conductor material due to its low resistivity (ρ_{Cu} = 1.67μΩ–cm) and its expected high electromigration resistance. Electroless-plated Cu has fine grains (the grain size is about 0.1 - 0.3μm) [23] and can be used as interconnects in high-resolution VLSI circuits. But the potential corrosion problem and the high diffusivity in oxide must be dealt with. Au is possibly less desirable because present electroless plating solutions start to decompose after usage [19], the thickness is limited to 0.25μm [20], and the grain size is too large (close to 1μm) [21].

The LOPED process can be easily modified to accommodate electroless plating. Instead of depositing the thick film (Fig.2.3(c)), a thin conductive film is deposited and patterned by the same process. This thin film, usually thinner than 0.1μm, can be either the catalytic material (Pd) or another conductive film (or films) to be activated later. For example in Cu deposition, a Ti film can be deposited and subsequently activated [21].

4.3 A Planarized Metallization Process Example

In this section a metallization process that can result in a completely planarized surface after the metal deposition and patterning is discussed and demonstrated experimentally. We focus on metal M2. The via-filling process will not be discussed since several methods have

been demonstrated, such as the tungsten plugs [9] and the electroless plating process [10]. The planarized interconnect process is discussed much less in the literature compared to the via-filling process, and only a few buried metal processes have been described [15,16]. In this section we discuss a buried metal process utilizing lift-off (LOPED) and SOG planarization [16].

Once a surface topography is created, it is extremely difficult to planarize the surface again without severely limiting the design rules (e.g. limited to a maximum metal space or a maximum metal width) as discussed in section 4.1. The only way to achieve complete planarity is to avoid the creation of topography. With the assumptions of the previous discussion, the only possible solution is D2 L2 M2 and its variations (Fig.4.6 - 4.11). The process flow for D2 L2 M2 is repeated in Fig.4.14. The LOPED lift-off process is used to pattern the metal film, and an additional step (Fig.4.14(e)) of applying a SOG film to smooth the remaining surface roughness is used.

After the vias are filled, a PECVD oxide film is deposited to between 0.8μm to 1.0μm thick. A layer of photoresist is coated and patterned by a dark-field metal mask on the oxide film(Fig.4.14(a)). A LAM plasma oxide etcher transfers the resist patterns into the oxide (Fig.4.14(b)), followed by a sputter-deposition of an Al-1%Si film in the CPA system (Fig.4.14(c)). The LOPED process is used to lift the resist and the excess metal film (Fig.4.14(d)). The process is completed by coating and curing a 200 nm SOG film over the surface (Fig.4.14(e)).

Examples of the cross-sections are shown in Fig.4.15. Two buried metal patterns separated by 1.0μm (Fig.4.15(a)) demonstrate the potential high-resolution of this process. The surface is flat after the SOG process as can be seen from both Fig.4.15(a) and Fig.4.15(b). With this process, the topography generated by the metal process is limited to that portion not compensated by the SOG film. The principle source derives from inability to deposit metal precisely to a thickness equal to the trench depth.

4.4 Some Future Work

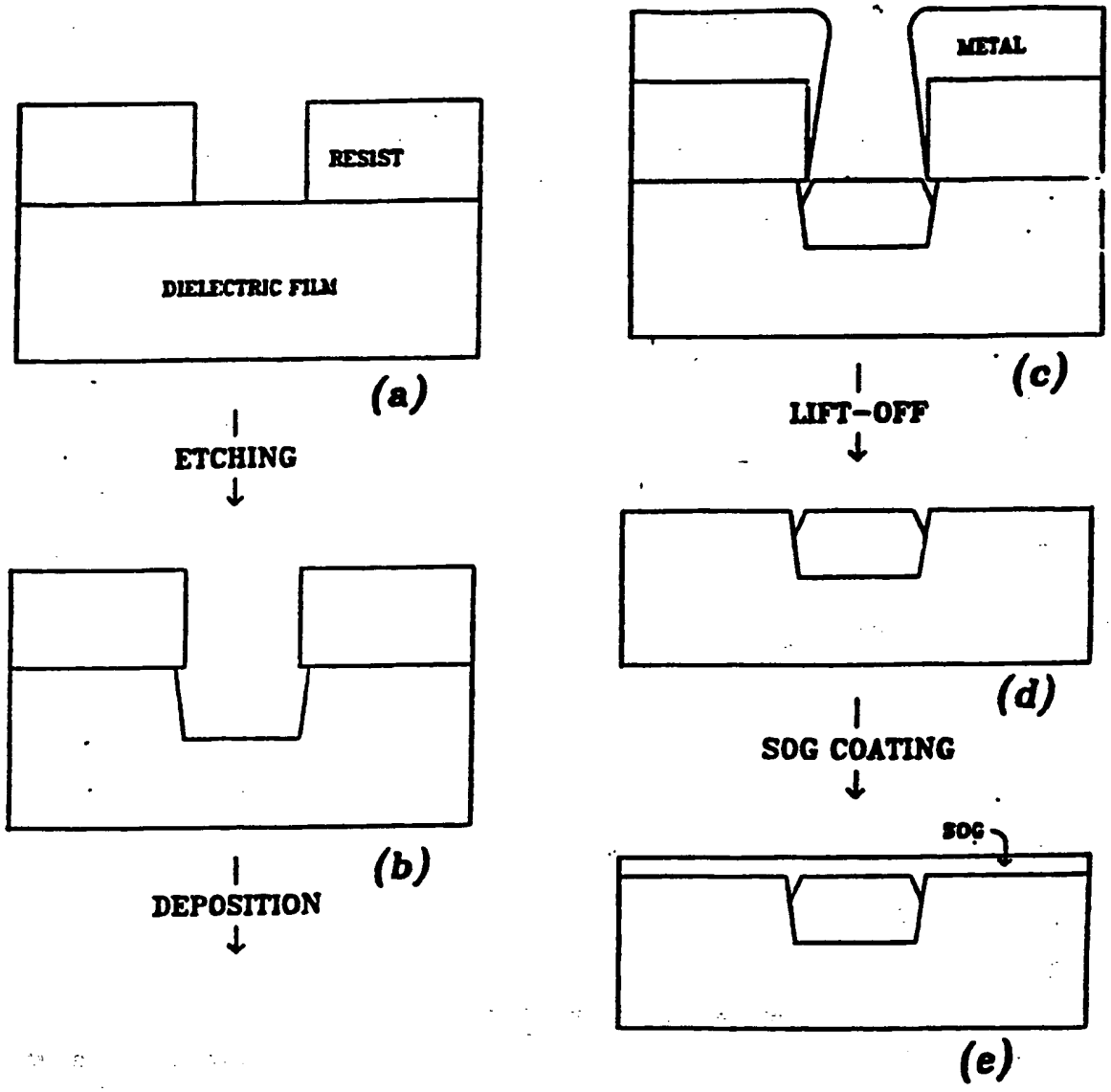
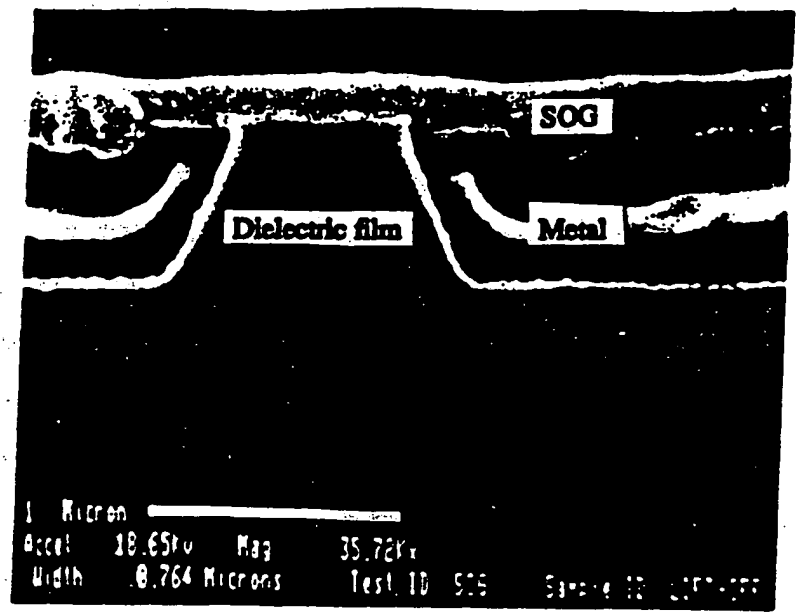
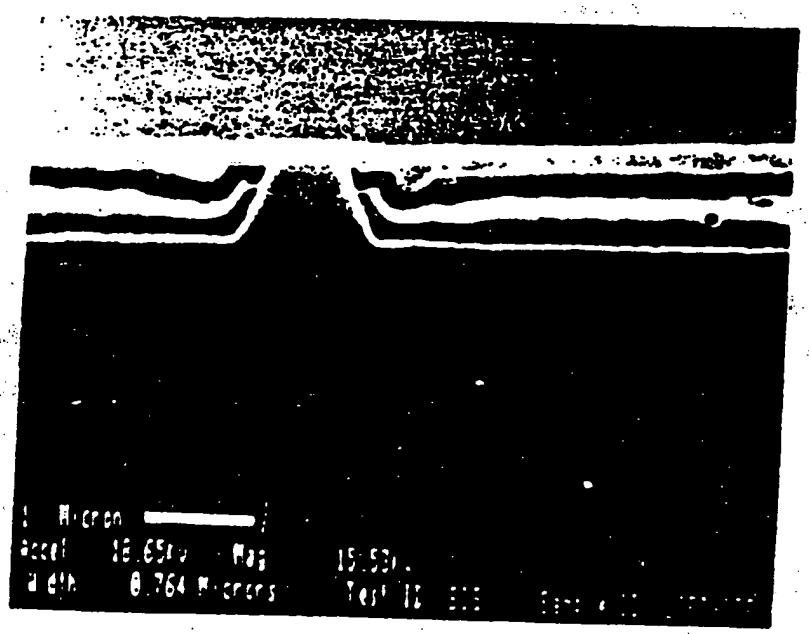


Fig.4.14 The process flow of a completely planarized metallization process. (a) A layer of photoresist is coated and patterned by a dark-field metal mask after the deposition of a thick oxide film. (b) An oxide etcher transfers the resist patterns into the oxide. (c) The metal film is sputter-deposited. (d) The LOPED process is used to remove the resist and the excess metal film. (e) The process is completed by coating and curing a 200 nm SOG film over the surface.



(a)



(b)

Fig.4.15 Examples of the buried metal process. (a) Two metal patterns (dark regions) are separated by 1.0μm. (b) With a smaller magnification, the planarity of the process is more evident.

In this section, some of the natural extensions of the previous work will be discussed. Referring to table 4.2, only the cases from Fig.4.6 to Fig.4.9 do not require planarization and can be extended to more than three or four layers. The D1 M1 D2 M2 approach (Fig.4.6) can simply repeat the DLM process using LOPED or electroless plating. The LOPED approach was presented in the last section; the electroless plating approach needs only slight modification to the LOPED process as presented in section 4.2. The cases of Fig.4.10 and Fig.4.11 require D1 planarization. If the vias are all small enough (e.g. less than 1μm), bias-sputtered quartz or spin-on glass can planarize the topography after via filling. Then the buried metal process in section 4.3 can be used for metal interconnects. In this section the D1 D2 M1 M2 case (Fig.4.7 to 4.9) will be discussed.

Referring to Fig.4.7, M1 can be deposited by lift-off or selective deposition. If lift-off is used, the high aspect ratios for the vias after L1 (Fig.4.7(c)) demands an extremely directional deposition for M1. Selective deposition is less sensitive to aspect ratio. In the deposition process the L1 resist is needed to cover the metal pattern areas (discussed with the M2 deposition process below), and the selective deposition process should not attack the resist. The electroless plating processes for Ni and Pd have a PH value between 6 and 9, and are preferred for M1 deposition.

M2 can only be deposited by a selective deposition process because the patterning medium does not exist during the process (Fig.4.7(d)). For the deposition to be selective, the areas to which the metal is deposited must be different from those "not-pattern" areas. In this case, both the "pattern" and "not-pattern" areas are the D2 dielectric film, and some process is needed after L2 before L1 to differentiate the pattern areas. If the electroless plating process is used, either a thin conductive film can be deposited or the surface can be activated by $PdCl_2$ solution after L2. The actual deposition process for M2 should not start prior to the completion of M1 deposition; otherwise, a topography about the depth of the vias may be created at the center of vias. The deposition is prevented by covering these metal pattern areas by L1 resist. After both M1 and M2 are deposited, a SOG film can aid in smoothing the remaining

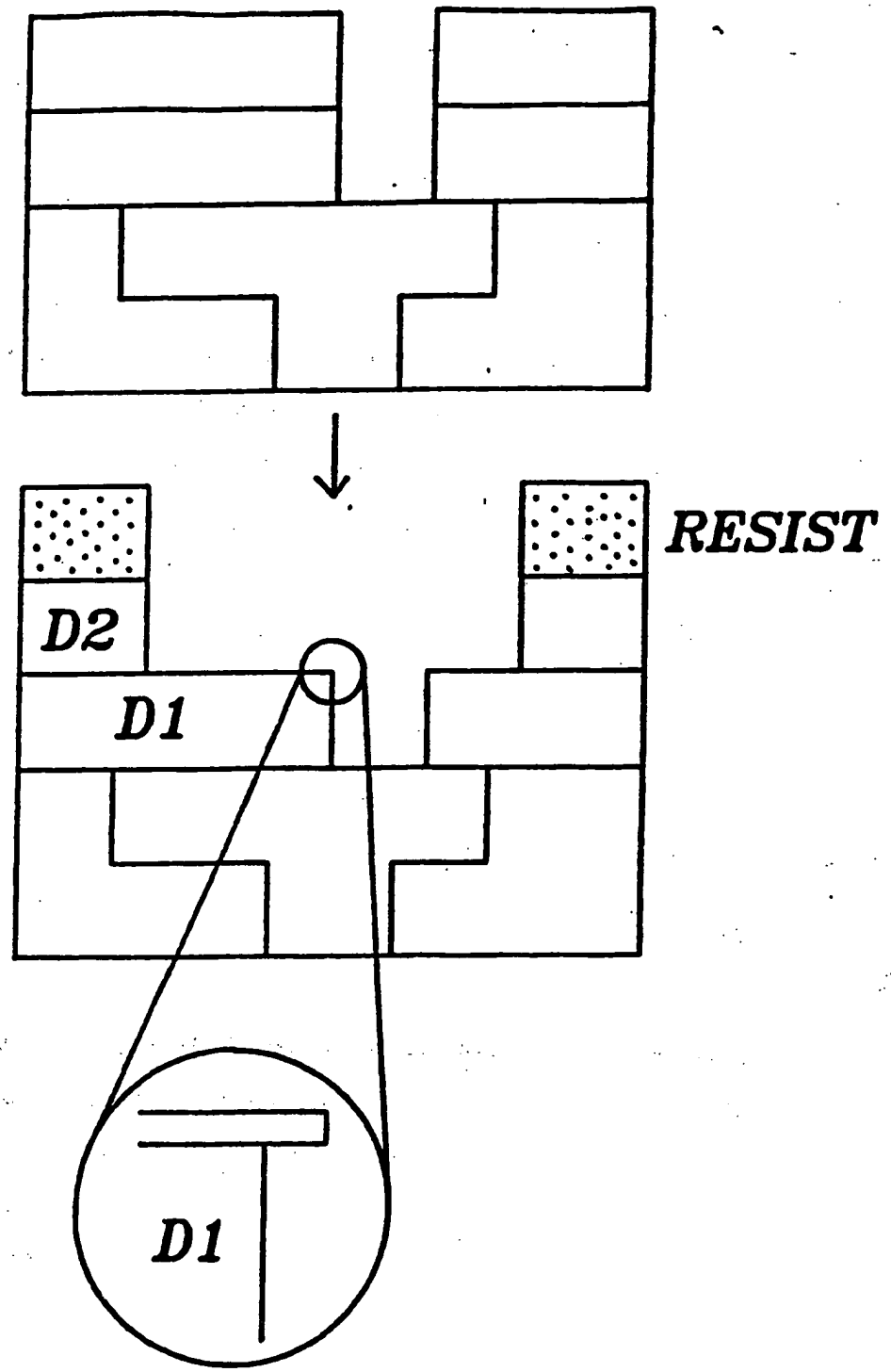


Fig.4.16 The potential difficulty with the D1 D2 L1 L2 M1 M2 process. After L1 opens the via through both D1 and D2, the L2 etching may under-cut the D1 under the interlayer between D1 and D2. It is exceedingly difficult to fill the areas under the overhang in the M1 deposition step.

surface roughness.

In the process described by Fig.4.8, the L2 patterning step (Fig.4.8(c)) requires extra care. As shown in table 4.2, a selective etching is needed between D1 and D2, or an "etch stop" is needed in between. If the L2 etching is not purely vertical, an undesirable overhang of the intermediate material may be created (Fig.4.16). A conformal deposition for M1 is desired to fill the space under the overhang. Electroless plating is known to be exceedingly conformal and is preferred in this case. The approach of using one deposition for both M1 and M2 (Fig.4.8a,b,c,e) may lead to topography formation over the vias. This topography is likely to result in step coverage problem for the following depositions.

The D1 D2 L1 M1 L2 M2 approach as in Fig.4.9 is straightforward and repetitive for M1 and M2. Here the electroless plating is also desirable for M1 and either LOPED or electroless plating can be used for M2.

From the previous discussion, it is concluded that in order to achieve more than three or four layers of metal films, the dielectric film must be deposited before the metal film, and a selective deposition process should be used to deposit the metal film. Electroless plating fits exceedingly well into the promising approaches.

4.5 Conclusion

The multilevel interconnection technology is examined in this chapter by dividing the process steps into six individual parts - D1, D2, M1, M2, L1, and L2. Under the assumptions used, there are in total 13 possible ways to construct a viable process sequence for each metal layer. Among all the possible ways, only four of them do not require planarization and are proposed as the most promising processes for VLSI and beyond. Two other processes require planarization for the vias. If the vias are small enough to be planarized easily, these two processed can also be used for the future.

All of the six processes require either selective deposition or lift-off to pattern the vias and the interconnects. Electroless plating is discussed as a low-temperature selective deposi-

tion process. Electroless-plated Pd and Ni are found to be suitable for via-filling, while electroless-plated Cu is well suited as the main interconnects material.

All of the six promising processes have D2 L2 M2 sequence for the interconnect patterns. Three of them can use lift-off, or LOPED, to pattern M2. It is shown that the combination of LOPED and SOG can provide an extremely flat surface and high resolution for the metallization process.

4.6 References

[1] D.W. Widmann, " Metallization of Integrated Circuits Using a Lift-Off Technique," *IEEE. J. Solid-State Cirsuits*, SC-11, 466(1976).

[2] M. Hatzakis, B.J. Canavello, J.M. Shaw, " Single-Step Optical Lift-Off Process," *IBM J. Res. Develop.*, 24, 452 (1980).

[3] A.A. Milgram, "Lift-Off Process for Achieving Fine-Line Metallization," *J. Vac. Sci. Technol.*, B1(2), 658 (1983).

[4] P.L. Pai, Y. Shacham-Diamand, W.G. Oldham, "High Resolution Additive Thin Film Patterning," *Kodak Microelectronic Seminar, Interface '85*, 127(1985).

[5] P.L. Pai, Y. Shacham-Diamand, W.G. Oldham, "A High Resolution Lift-Off Technology for VLSI Interconnections," *VLSI Multilevel Interconnection Conf.*, 209(1986).

[6] T.D. Bonifield, R.J. Gale, B.W. Shen, G.C. Smith, C. Huffman, " A One Micron Design Rule Double Level metallization Process," *VLSI Multilevel Interconnection Conf.*, 71(1986).

[7] M.J. Thoma, W.T. Cochran, A.S. Harrus, H.P. Hey, G.W. Hills, C.W. Lawrence, J.L. Yeh, " A 1.0 Micrometer CMOS Two Level Metal Technology Incorporating Plasma Enhanced TEOS," *VLSI Multilevel Interconnection Conf.*, 20(1987).

[8] T.A. Bartush, " A Four Level Wiring Process for Semiconductor Chips," *VLSI Multilevel Interconnection Conf.*, 41(1987).

[9] T. Moriya, S. Shima, Y. Hazuki, M. Chiba, M. Kashiwaga, " A Planar Metallization Process-Its Application to Tri-Level Aluminum Interconnection," *1983 IEDM*, 550 (1983).

[10] Y. Harada, K. Fushimi, S. Madokoro, H. Sawai, S. Ushio, " The Characterization of Via-Filling Technology with Electroless Plating Method," *J. Electrochem. Soc.*, 133(11), 2428 (1986).

[11] T.O. Herndon, J.A. Burns, G.H. Chapman, " Planar Vias by Ion Implantation," *VLSI Multilevel Interconnection Conf.*, 103(1987).

[12] P.L. Pai, W.G. Oldham, Chiu H. Ting, Milan Paunovic, " A Planarized Metallization Process Using Selective Electroless Deposition And Spin-On Glass," *ECS Fall Meeting*, (1987).

[13] E.R. Sirkin, I.A. Blech, " A Method of Forming Contacts Between Two Conducting

Layers Separated by a Dielectric," *J. Electrochem. Soc.*, 131(1), 123(1984).

[14] M.T. Welch, C. Garcia, " Pillar Interconnections for VLSI technology," *VLSI Multilevel Interconnection Conf.*, 450, (1986).

[15] S Wong, *IEDM Tech. Digest*, (1986).

[16] P.L. Pai, W.G. Oldham, "Metallization Approaches Using Lift-off and Spin-on Glass," *the 1987 International Symposium on VLSI Technology, System and Applications*, 187, (1987).

[17] I. Ohno, O. Wakabayashi, S. Haruyama, " Anodic Oxidation of reductants in Electroless Plating," *J. Electrochem. Soc.*, 132(10), 2323(1985).

[19] Luby Ramankiw (IBM Corp.), *private communications.*

[20] EL-221 Gold Plating solution data sheet, Shipley.

[21] M. Paunovic (Intel Corp.), *private communications.*